Design of a High Efficiency High Power Density DC/DC Converter for Low Voltage Power Supply in Electric and Hybrid Vehicles

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Conception d'un Convertisseur à Haut Rendement et Très Forte Puissance Massique pour Alimentation du Réseau de Bord Basse Tension des Véhicules Electriques et Hybrides

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Conception d'un Convertisseur à Haut Rendement et Très Forte Puissance Massique pour Alimentation du Réseau de Bord Basse Tension des Véhicules Electriques et Hybrides

Résumé

Cette thèse traite de la conception d'un convertisseur DC / DC destiné aux véhicules électriques et hybrides (2,5 kW, 400V/14V, 250kHz). Dérivé de la topologie LLC à résonance, ce convertisseur bénéficie des nombreux avantages propres à cette structure particulière. C'est ainsi que le prototype réalisé présente un rendement très élevé, une densité de puissance très forte avec des perturbations EMI très réduites. La première partie de cette thèse est consacrée à l'analyse théorique du circuit LLC afin de dégager un modèle de conversion et une stratégie de contrôle adaptée à l'application visée. Afin de conserver un rendement important sur une large plage de charge, une structure basée sur la mise en parallèle de deux modules LLC est proposée. Une nouvelle stratégie de contrôle à deux boucles est également proposée pour équilibrer le courant entre les deux modules. La seconde partie de la thèse fait appel à la simulation et à l'expérimentation. Il s'agit de minimiser la masse et l'encombrement tout en maximisant le rendement. Un composant magnétique spécial est conçu puis dimensionné pour intégrer le transformateur et diverses inductances. Pour cela, les pertes dans le circuit magnétique et les enroulements sont quantifiées en fonction de divers modes de réalisation et diverses géométries. Ce convertisseur met également en œuvre un système de redressement synchrone robuste avec une compensation de phase, un module de puissance avec une résistance thermique très faible et un système de refroidissement efficace par air. Le rendement maximal mesuré est 95%. Le rendement demeure supérieur à 94% sur une plage de puissance s'étalant de 500 W à 2 kW. La densité de puissance est 1W/cm3. La CEM du convertisseur est développée dans cette thèse.

Mots-clés: convertisseur à résonance LLC, commutation douce, composant magnétique, augmentation du rendement, équilibrage de courant

Design of a High Efficiency High Power Density DC/DC Converter for Low Voltage Power Supply in Electric and Hybrid Vehicles

Abstracts

In this dissertation, a 2.5kW 400V/14V, 250kHz DC/DC converter prototype is developed targeted for electric vehicle/hybrid vehicle applications. Benefiting from numerous advantages brought by LLC resonant topology, this converter is able to perform high efficiency, high power density and low EMI. A first part of this dissertation is the theoretical analysis of LLC: topology analysis, electrical parameter calculation and control strategy. To arrange high output current, this thesis proposes parallel connected LLC structure with developed novel double loop control to realize an equal current distribution. The second part concerns on the system amelioration and efficiency improvement of developed LLC. A special transformer is dimensioned to integrate all magnetic components, and various types of power losses are quantified based on different realization modes and winding geometries to improve its efficiency. This converter also implements a robust synchronous rectification system with phase compensation, a power semiconductor module, and an air-cooling system. The power conversion performance of this prototype is presented and the developed prototype has a peak efficiency of 95% and efficiency is higher than 94% from 500W to 2kW, with a power density of 1W/cm^3. The CEM analysis of this converter is also developed in this thesis.

Keywords: LLC resonant converter, soft switching, magnetic components, efficiency improvement, current sharing

To my family:

My parents: Mr. Xiaoping YANG and Ms. Jie WANG

My fiancée: Miss. Qian WANG

To my tutors:

Prof. Daniel SADARNAC

Mr. Patrick DUBUS

And all the other comrades who contributed …

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RESUME

La principale source d'alimentation des futurs véhicules électriques sera généralement une batterie haute tension, de tension comprise entre 220V et 410V. Elle permettra essentiellement le pilotage de la chaîne de traction. Le choix d'une tension de batterie beaucoup plus élevée qu'actuellement s'explique par la puissance électrique à fournir (entre 15kW et 100kW selon le type de véhicule) et l'autonomie recherchée (variant de 100km à 400km selon les cahiers des charges). Pour des problèmes liés à la sécurité des personnes, ce réseau HT sera confiné dans une partie du véhicule et limité aux équipements de traction ou de forte puissance. En ce qui concerne les autres fonctions à assurer dans le véhicule, l'alimentation se fera via le réseau BT classique 14V (variant entre 12V et 16V).

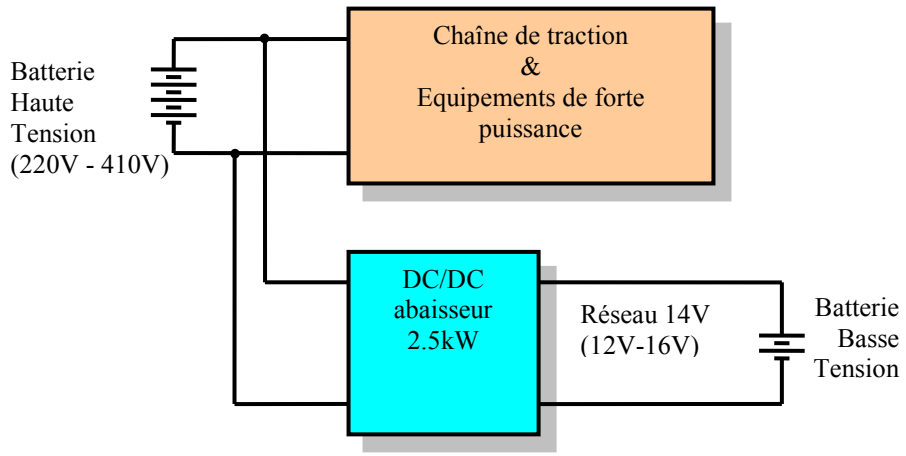


Figure R-1. Chaine de traction électrique dans un véhicule électrique ou hybride

Tous les véhicules électriques (ou hybrides) seront équipés d'un convertisseur DC/DC abaisseur générant une tension 14V à partir de la batterie haute tension (figure R-1). Une seconde batterie 14V sera également connectée sur ce réseau pour les phases de démarrage, d'arrêt et de diagnostique (la batterie haute tension n'étant pas activée durant ces phases). Il est important d'innover pour la réalisation de cette fonction afin d'optimiser le rendement, le volume et les performances. Dans les véhicules électriques/hybrides, ce convertisseur DC/DC doit pouvoir fonctionner à n'importe quelle puissance, de 0 à 2.5kW. Cependant, il y a deux gammes de puissance particulièrement utilisées : 600-900W et 1,5k-1,8kW. Assurer un rendement de conversion plus élevé dans ces deux domaines de puissance est très important afin d'améliorer les performances globales du convertisseur.

Le convertisseur LLC, dont la topologie est présentée à la figure R-2, se développe rapidement à l'heure actuelle dans les systèmes de conversion d'énergie de type 'front-end'. Le convertisseur LLC permet de réaliser des commutations à zéro de tension (ZVS) au niveau des interrupteurs primaires et des commutations à zéro de courant (ZCS) au niveau des interrupteurs secondaires. Cela permet d'augmenter beaucoup la fréquence de découpage par rapport à celle des convertisseurs MLI (PWM) traditionnels. Le circuit résonnant comprend deux inductances et un condensateur. L'inductance de magnétisation du transformateur peut être utilisée pour réaliser l'inductance Lm. De la même façon, l'inductance de fuite du transformateur est utilisable pour réaliser totalement ou partiellement l'inductance de résonance. Le volume global des composants magnétiques peut être donc réduit, ce qui présente un très grand avantage du convertisseur LLC par rapport à d'autres types de convertisseurs.

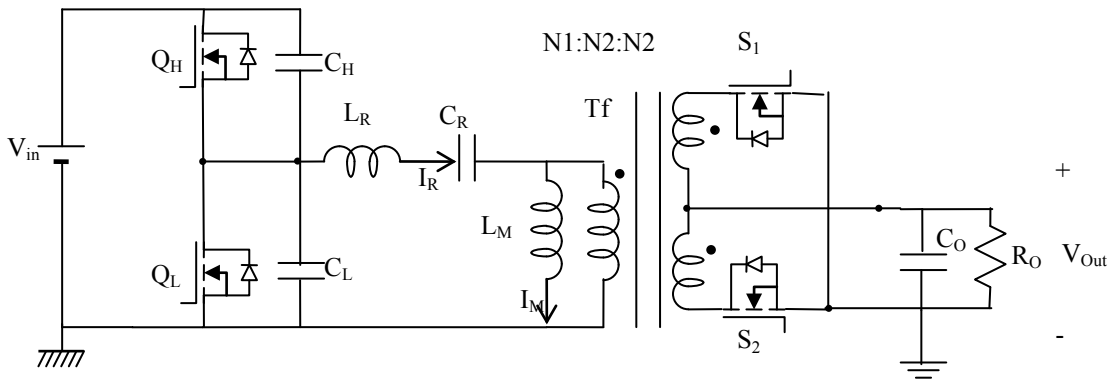


Figure R-2. Convertisseur LLC en forme de demi-pont avec redressement synchrone

Etude théorique :

Le choix d'un convertisseur à résonance LLC lors de la conception des alimentations DC/DC de puissance faible ou moyenne, dans les applications HT/BT, se traduit généralement par un très bon rendement. En général, les convertisseurs LLC mentionnés dans les publications sont de puissance inférieure à 1kW, souvent comprise entre 300W et 1kW. Une puissance supérieure mène à deux difficultés majeures :

Le premier problème réside dans la réalisation du transformateur. L'inductance magnétisante du transformateur nécessaire dans le circuit LLC est proportionnelle à la résistance de charge. Pour le convertisseur LLC de 2,5 kW, la charge équivalente est de 80mΩ. La valeur Lm requise est trop basse pour être réalisée en utilisant classiquement un noyau magnétique à entrefer. L'entrefer serait en effet beaucoup trop large, ce qui entrainerait notamment un flux

de fuite important vers les enroulements et donc des pertes supplémentaires par courants de Foucault. En comparaison pour un convertisseur LLC de puissance moitié, soit 1.25kW, l'inductance de magnétisation du transformateur requise est doublée et la largeur d'entrefer devient plus raisonnable.

La deuxième difficulté est l'augmentation très rapide des pertes par conduction dans les semi-conducteurs et dans le transformateur en fonction de la puissance du convertisseur. Le courant efficace dans les MOSFETs primaires et secondaires d'un convertisseur LLC de 2,5 kW est deux fois plus élevé que dans un convertisseur LLC de 1.25kW. Afin de réduire les pertes globales par conduction, plusieurs transistors MOSFET doivent être connectés en parallèle. La section des enroulements du transformateur devant également être augmentée, il en résulte un volume supérieur de circuit magnétique, ce qui rend encore plus difficile d'obtenir une faible inductance magnétisante.

Nous avons retenu le convertisseur de type LLC compte tenu de ses caractéristiques intéressantes pour l'application visée. Cependant, pour pallier aux problèmes dus à l'augmentation de puissance, il est intéressant de réaliser le convertisseur sous la forme de plusieurs modules LLC fonctionnant en parallèle et se partageant le courant total. Nous avons opté pour l'utilisation de deux modules.

Le convertisseur LLC à deux cellules entrelacées, connectées en parallèle au primaire comme au secondaire est connu d'après la bibliographie comme un bon candidat pour gérer la forte puissance. Les principes décrits dans les publications font état de deux modules fonctionnant simultanément à une même fréquence. Les deux modules sont commandés par un même contrôleur imposant un déphasage de 90° entre eux de manière à minimiser le contenu harmonique des courants d'entrée et de sortie du convertisseur global. Cela fonctionne parfaitement si les deux circuits résonnants sont identiques. Cependant, la dispersion des valeurs de composants entraîne une répartition aléatoire de courant entre les deux cellules.

Afin d'équilibrer correctement les transferts d'énergie entre les deux modules et de leur faire partager équitablement les contraintes, notamment les pertes, nous proposons dans cette thèse une autre solution pour commander ce convertisseur LLC parallèle-parallèle. La nouvelle méthode de contrôle fait appel à deux boucles de régulation : une boucle externe pour la tension de sortie et une boucle interne pour le courant d'entrée. L'équilibrage de courant entre les deux modules en parallèle est assuré en contrôlant le courant d'entrée de chaque cellule. La mesure des courants d'entrée est assurée par un shunt résistif pour raison de simplicité. La

figure R-3 montre le convertisseur LLC proposé à double phase et avec les deux capteurs de courant RA et RB à l'entrée de chaque cellule. Le capteur de courant est placé entre la cellule de puissance et la masse primaire de manière à ce que la mesure de courant ne soit pas flottante.

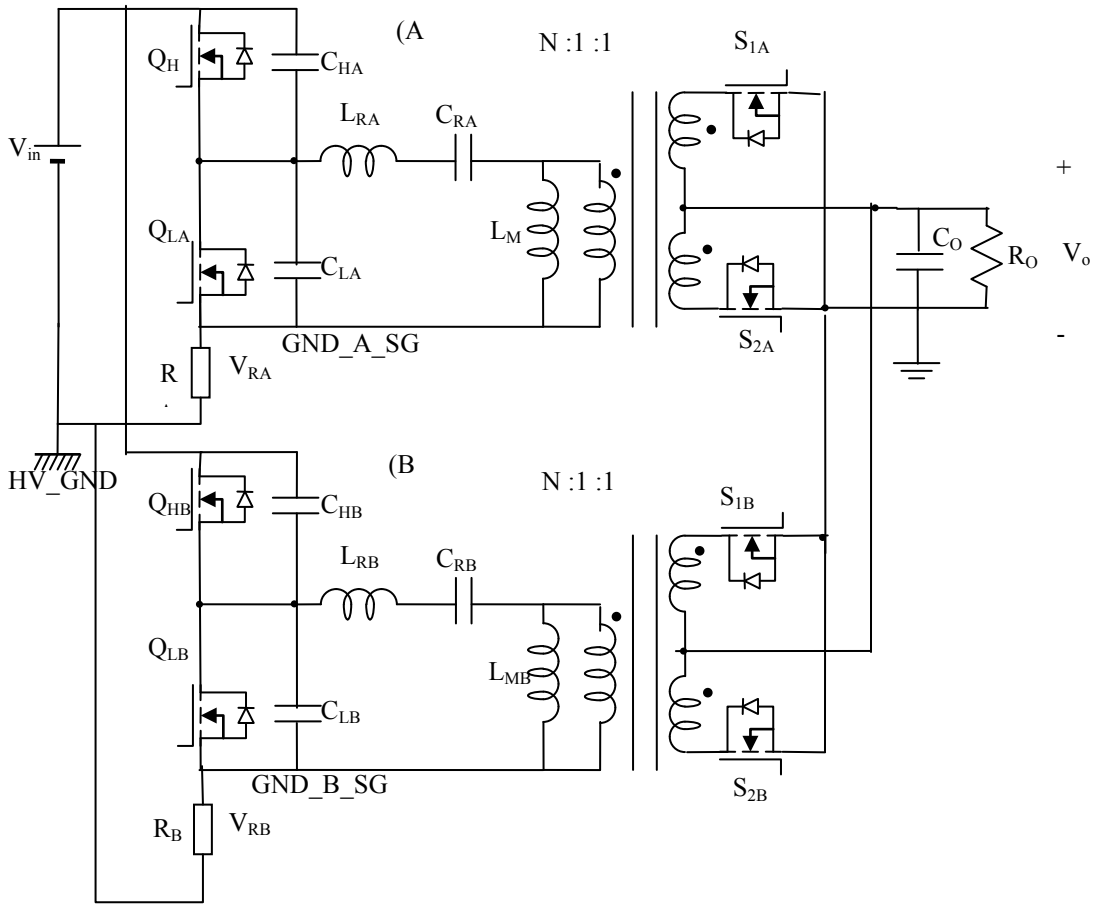


Figure R-3. Convertisseur LLC à double phase proposé avec capteurs de courant

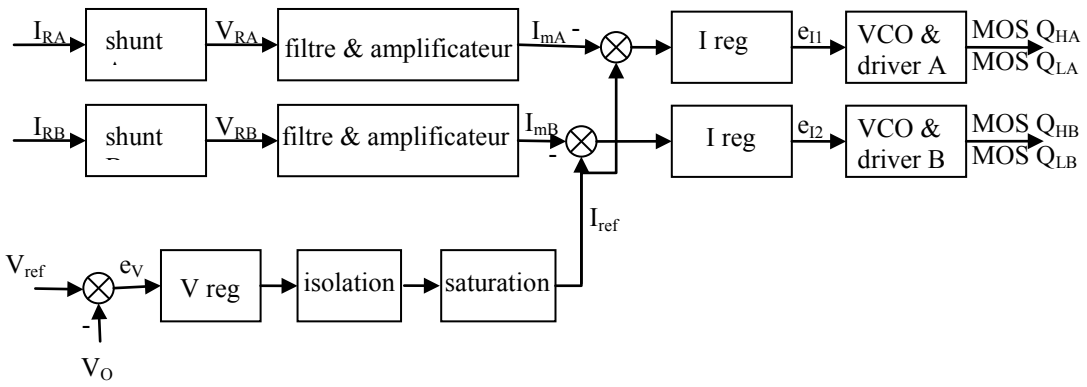


Figure R-4. Schéma-bloc du circuit de commande pour équilibrer les courants entre les deux modules LLC du convertisseur

Le schéma-bloc du circuit de commande proposé pour équilibrer les courants entre modules, adapté au convertisseur LLC à double phase, est présenté à la figure-R4. Le shunt R_A de la cellule de puissance A et le shunt R_B de la cellule de puissance B renvoient les signaux de courant d'entrée sous forme de tensions distinctes V_{RA} et V_{RB}. Après filtrage et amplification à un niveau approprié, ces signaux sont notés I_{mA} et I_{mB}. Ils reflètent les valeurs moyennes des courants en entrée de chaque cellule. Le filtre réalise une caractéristique de type passe-bas avec une forte atténuation dans la gamme de fréquence opérationnelle du convertisseur. En ce qui concerne la boucle externe de régulation de la tension de sortie, celle-ci est comparée à la tension de référence, puis l'erreur de comparaison e_V est soumise à un régulateur de tension du type PI. La régulation de tension fournit la référence de courant $I_{ref,}$ unique pour les deux cellules de puissance. Cette référence I_{ref} doit être isolée de la partie BT et limitée à une certaine valeur pour éviter toute surintensité. Les images I_{mA} et I_{mB} des courants sont asservis à la référence I_{ref} par le régulateur de courant respectif à chaque cellule. C'est ainsi que l'équilibrage des courants d'entrée entre les deux cellules de puissance peut être assuré. Les signaux e_{I1} et e_{I2} sont envoyés à deux oscillateurs (des oscillateurs contrôlés en tension de type VCO ou des oscillateurs contrôlés en courant de type ICO). Des drivers permettent de commander correctement les MOSFETs du demi-pont.

Il est important de remarquer que les deux convertisseurs fonctionnent ainsi à deux fréquences légèrement différentes afin de maintenir le même ratio de conversion de tension. La différence de fréquences provient de la dispersion des valeurs de composants dans les deux circuits résonnants. L'analyse des conséquences de cette double fréquence de découpage fait partie de cette thèse.

Le logiciel Simplis est utilisé pour étudier la fonction de transfert du convertisseur LLC et désigner les paramètres des régulations. La modèle dynamique du convertisseur à résonance en régime de faible amplitude est difficile à obtenir par la méthode de l'état moyenné. Le logiciel Simplis intègre une analyse périodique du point de fonctionnement (POP analysis) qui permet de déterminer la fonction de transfert du convertisseur LLC sans établir son modèle à faible signal. Grâce aux résultats obtenus par simulation, nous avons pu déterminer les paramètres de régulation pour obtenir un système rapide, stable et précis, comme l'atteste la figure R-5.

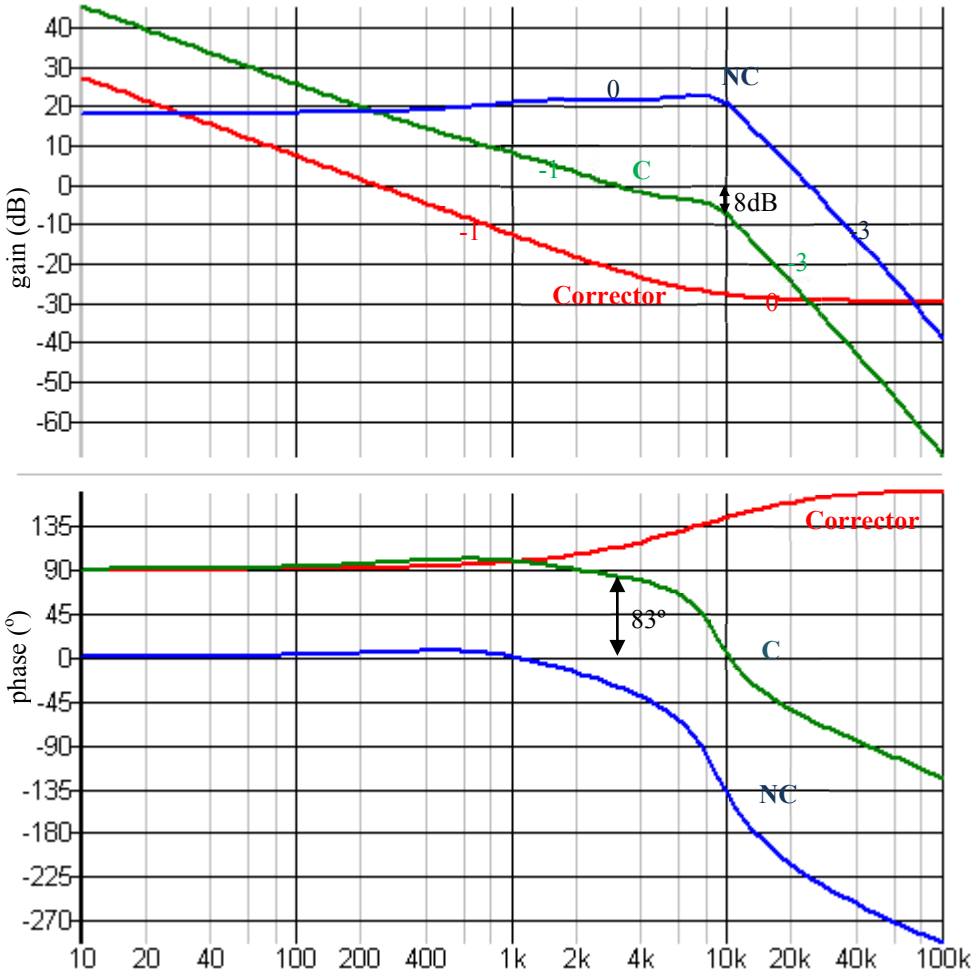


Figure R-5. Diagramme de Bode de la fonction de transfert en boucle ouverte non corrigée (NC) et corrigée (C) à P=1250W et Vin=330V pour la boucle interne de courant

Pour la boucle de courant, après correction, la bande passante obtenue est de 3kHz, avec une marge de phase de 83º et une marge de gain de 8dB. La même simulation est faite pour la boucle externe de tension, avec les résultats de la figure R-6.

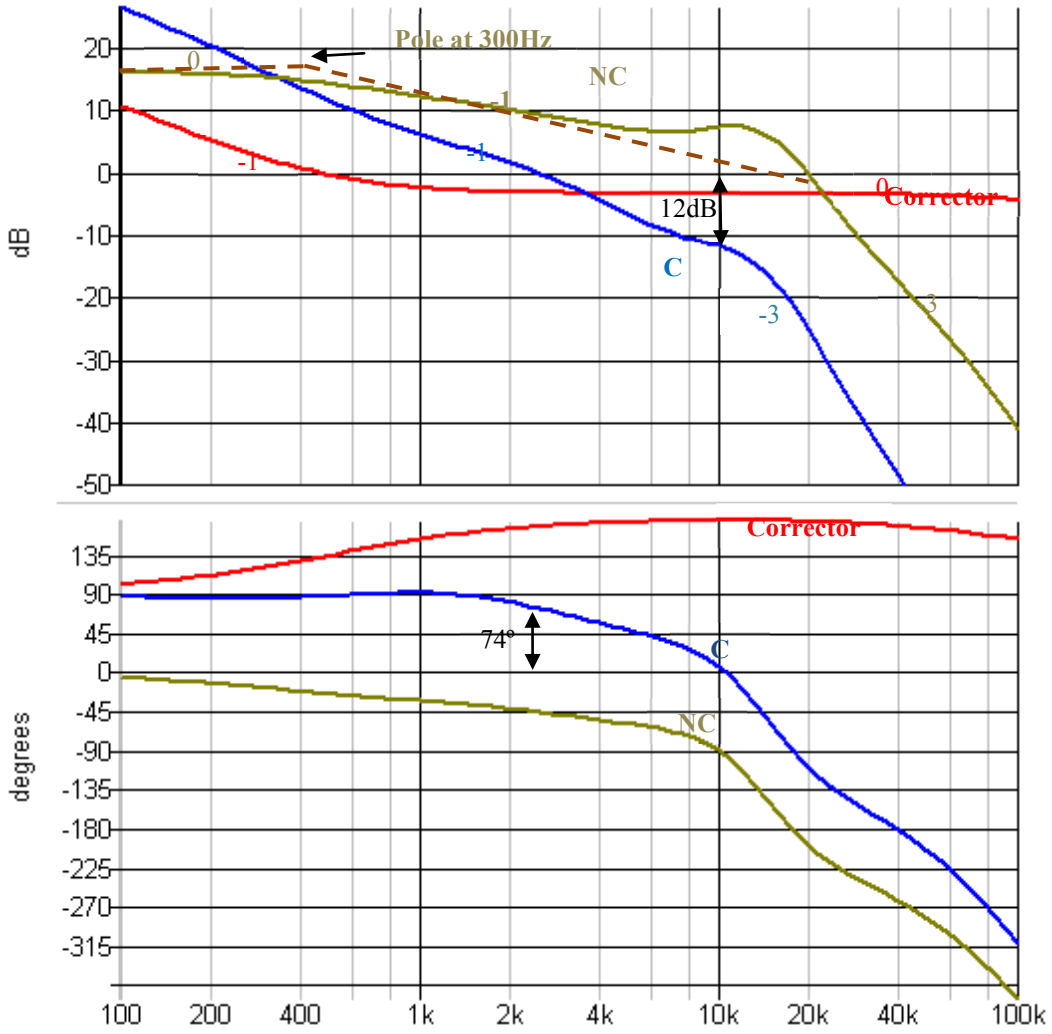


Figure R-6. Diagramme de bode de la fonction de transfert en boucle ouverte non corrigée (NC) et corrigée (C) à P=1250W et Vin=330V pour la boucle externe de tension

Pour le boucle de tension, après correction, la bande passante obtenue est de 2.5kHz, avec une marge de phase de 74º et une marge de gain de 12dB.

En outre, le convertisseur de LLC est capable de réaliser la fonction de démarrage progressif (soft-start), la protection en cas de surcharge ou de court-circuit, la protection en cas de surtension…

Concernant le dimensionnement du circuit LLC, afin d'obtenir une grande plage de variation de tension en entrée avec une plage de fréquence de fonctionnement limitée, une faible valeur est nécessaire pour l'inductance Lm. À cause de cette faible inductance, le courant de magnétisation est important en regard du courant de résonance, ce qui tend à dégrader le rendement global. Le moyen le plus efficace pour améliorer le facteur de puissance des bras

de pont est d'augmenter le plus possible l'inductance magnétisante Lm. Cependant, la plage de variation de tension en entrée doit alors être réduite. En particulier, une inductance Lm trop forte abaisse trop le gain statique du convertisseur et le rend inapte à fonctionner sous la tension minimale de 220 V en entrée. En conséquence, un convertisseur de type BOOST doit alors être placé en amont du convertisseur LLC, comme à la figure R-7.

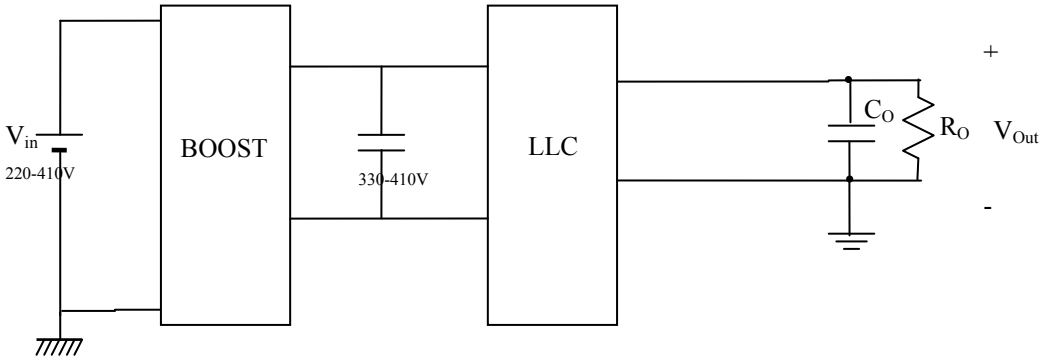


Figure R-7. Double étage LLC+BOOST pour améliorer le rendement global

Comme indiqué sur la figure R-7, la plage de variation de la tension en entrée du convertisseur LLC est réduite à 330-410V. Pour une tension en entrée du système global Vin inférieure à 330 V, le convertisseur BOOST est activé pour augmenter la tension jusque vers 330V. Pour Vin supérieure à 330 V, le convertisseur BOOST est désactivé de manière à appliquer directement la tension d'entrée au convertisseur LLC (seule la diode du BOOST conduit alors). La limite de 330 V est choisie en fonction des caractéristiques de charge de la batterie dans les véhicules électriques (figure R-8).

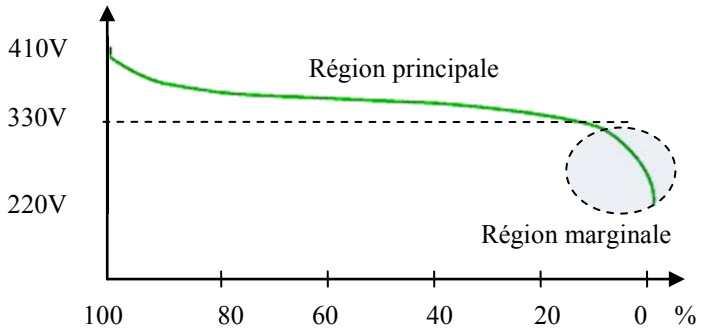


Figure R-8. Etat de charge d'une batterie au lithium-ion dans les véhicules électriques

D'après la figure R-8, la plage de fonctionnement de [220V 330V] correspond en fait à un domaine de fonctionnement marginal du convertisseur. Ainsi, la plupart du temps, le

convertisseur BOOST n'est pas activé. La comparaison des performances, avec et sans BOOST, fait partie de cette thèse. C'est ainsi que le BOOST permet d'augmenter le rendement global d'au moins 2% dans la gamme de tension [330V 410V] et d'au moins 1% dans la gamme [220V 330V]. Durant la thèse, les travaux ont porté essentiellement sur la conception du convertisseur LLC, ce qui a permis de réaliser et d'optimiser un prototype toutefois sans BOOST.

L'approximation dite « du premier harmonique » (FHA) est une méthode simplifiée permettant d'analyser beaucoup de convertisseurs à résonance. Elle permet en particulier d'établir le circuit électrique équivalent d'un convertisseur LLC en approchant les formes de courant et de tension par une forme sinusoïdale tout en négligeant les effets des autres harmoniques d'ordre plus élevé. Dans l'analyse traditionnelle du convertisseur LLC, l'effet de l'inductance de fuite partielle au secondaire du transformateur (et de l'inductance de câblage secondaire) est négligé. Toutefois, à fréquence suffisamment élevée et en cas de fort courant et faible tension en sortie, l'impédance de cette inductance parasite devient non négligeable devant la charge nominale : l_2=120nH, soit 116mΩ à 150kHz, comparable à la charge de 160mΩ. Son effet doit être donc pris en compte dans la conception et le dimensionnement du convertisseur. La figure R-9 représente les circuits équivalents d'une cellule de résonance LLC idéalisée et d'une cellule comprenant l'inductance parasite précédente.

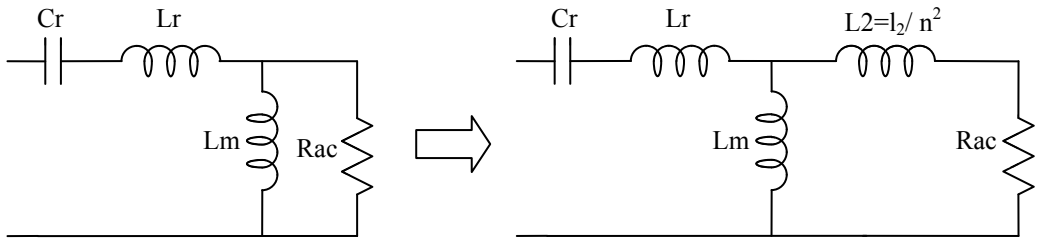


Figure R-9. Les circuits équivalents d'une cellule de résonance LLC idéalisée et d'une cellule avec l'inductance parasite ramenée au primaire

L'étude analytique par la méthode du premier harmonique d'un convertisseur LLC doté d'une cellule de résonance idéale (figure R-9(1)) mène à un ratio de conversion normalisé donné par la relation R-1 :

$$G = \frac{1}{\left(1 + \lambda - \lambda \frac{1}{f_n^{\,2}}\right) + jQ\left(f_n - \frac{1}{f_n}\right)} \quad \text{(R-1)}$$

Dans cette expression : $Q = \frac{\sqrt{L_r / C_r}}{R_{ac}}$ est le facteur de qualité ; $f_n = \frac{f_s}{f_r}$ est la fréquence de découpage normalisée ; $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$ est la fréquence de résonance principale ; $f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}$ est la fréquence de résonance secondaire ; $\lambda = \frac{L_r}{L_m}$ est le ratio entre l'inductance de résonance et l'inductance magnétisante.

En considérant l'effet de l'inductance de fuite secondaire avec $L_2 = \frac{l_2}{n^2}$, le ratio de conversion normalisé du convertisseur LLC est donné par la relation R-2 :

$$G = \frac{1}{\left(1 + \lambda - \lambda \frac{1}{f_n^{\,2}}\right) + jQ\left(\left(\frac{L_2}{L_m}\left(1 + \frac{1}{\lambda}\right) + 1\right) f_n - \left(\frac{L_2}{L_m} + 1\right)\frac{1}{f_n}\right)} \quad \text{(R-2)}$$

La figure R-10 montre la différence entre les deux ratios.

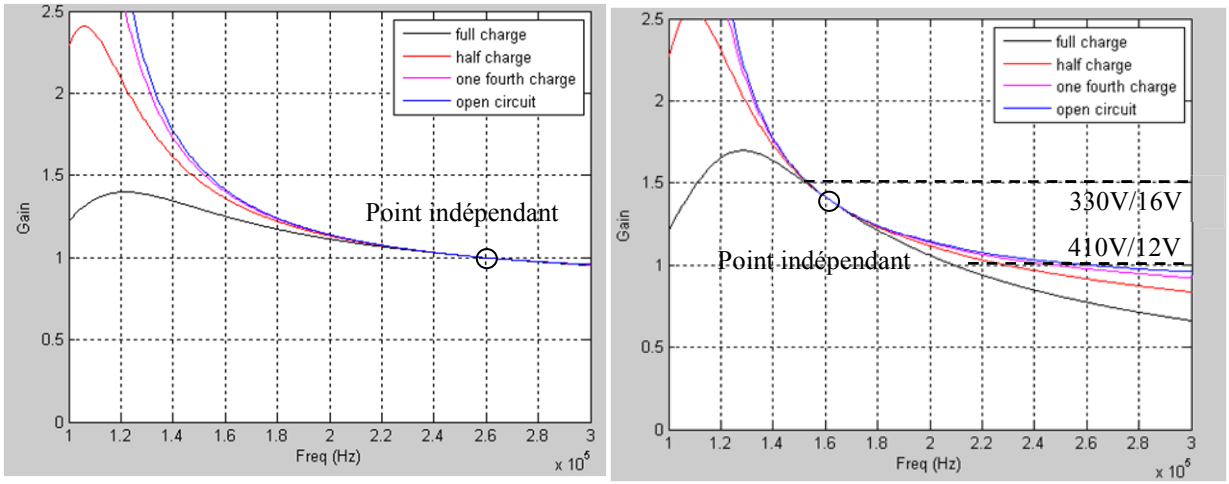


Figure R-10. Caractéristiques des cellules LLC idéale (Lr=7.5uH, Cr=50nF, Lm=42µH) et non-idéale (avec l_2=120nH)

Plusieurs conclusions relatives à la présence de L_2 peuvent être tirées de ce qui précède :

(1) En l'absence de charge, Q = 0, le gain reste le même que dans le convertisseur LLC idéal.
(2) La fréquence de résonance principale ne correspond plus à un gain indépendant de la charge. Le gain à la fréquence de résonnance est toujours inférieur ou égale à 1.
(3) Le point indépendant de la charge est déplacé vers une fréquence inférieure $f_{ind} = \frac{1}{2\pi\sqrt{C_r(L_r + L_m // L_2)}}$, avec un gain supérieur à 1, $G_{f=find} = \frac{L_m + L_2}{L_m}$.

(4) Pour une même valeur de Q, le taux de conversion maximal est augmenté.

En conclusion, le dimensionnement des deux modules LLC doit prendre en compte toutes les inductances de fuite partielles du transformateur et les inductances de câblage. Comme indiqué sur la figure R-10, le convertisseur LLC est conçu pour fonctionner avec une tension d'entrée de 330-410V et une tension de sortie 12-16V. La fréquence de fonctionnement est alors comprise entre 150 kHz et 260kHz. Toutefois, afin de simplifier les tests du prototype, la tension de sortie a été régulée à une valeur constante de 14 V en présence d'une charge purement résistive, variable dans de grandes proportions (0 à 2.5 kW).

Réalisation pratique et expérimentation

Un point critique concerne les pertes énergétiques dans la partie secondaire, notamment dans les MOSFETs des redresseurs synchrones, à cause du courant de sortie très intense sous basse tension. Les MOSFETs standards, sous forme d'éléments discrets, sont difficiles à utiliser ici en raison de leur conductivité thermique limitée et de leur résistance d'interconnexion. Plusieurs MOSFETs devraient être connectés en parallèle afin de résoudre ce problème, ce qui augmenterait le nombre global de semi-conducteurs et l'encombrement global. Nous avons plutôt opté pour un module de puissance dédié intégrant tous les MOSFETs BT.

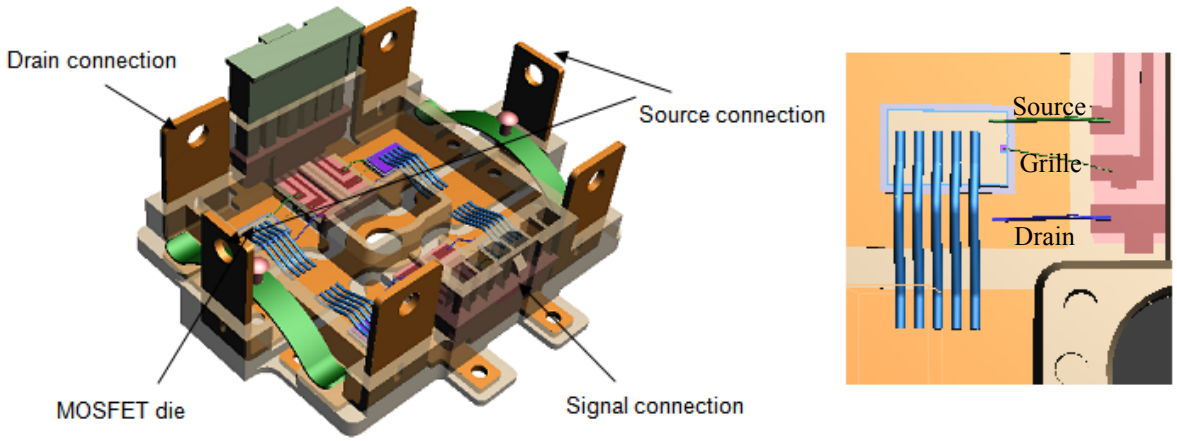


Figure R-11. Intégration des 4 MOSFETs BT « nus » dans le module de puissance IML

Dans le cadre de notre projet, un module de puissance du type 'lead-frame inséré surmoulé (IML) a été conçu. Il est représenté à la figure R-11. Les lead-frames sont insérés dans une pièce moulée en matière plastique qui présente des zones ouvertes horizontales dans lesquelles les puces nues de MOSFETs sont brasées. Les lead-frames supportent donc les

puces, et s'étendant aussi vers l'extérieur, ils forment également les bornes de connexion électrique. Le module de puissance conçu est composé de quatre puces nues formant une configuration à double phase. Les quatre sources des puces sont connectées ensemble (voir la figure R-3) et vers le lead-frame par des liaisons 5x500µm. Afin d'effectuer la rectification synchrone, les connexions de signal sont réalisées par les liaisons 125µm. Le module de puissance lui-même est fixé à la plaque de refroidissement par des vis. Le lead-frame est constitué de cuivre de 0,8 mm d'épaisseur permettant ainsi une bonne conductivité électrique et thermique. La puce nue choisie est fournie par Infineon : IIPC22S4N06. Elle présente une résistance interne Rdson = 1.3mΩ , une charge de grille Qg = 208nC et une tension VDSS = 60V. La résistance totale, y compris celle du lead-frame, est inférieure à 2mΩ. La résistance thermique totale, y compris celle des interfaces thermiques, est Rth=1.393 ºC/W.

L'inductance magnétisante nécessaire est Lm = 42uH. La réalisation ne pose pas de problème : pour 16 tours du côté primaire du transformateur, un noyau magnétique possédant une faible inductance spécifique AL, de l'ordre de 165nH, doit être utilisé (ex : avec entrefer). Une inductance de fuite suffisante pour réaliser une inductance de résonance impose de séparer les enroulements secondaires du primaire. La solution retenue consiste à intercaler les 16 spires du primaire entre les enroulements secondaires, comme à la figure R-12.

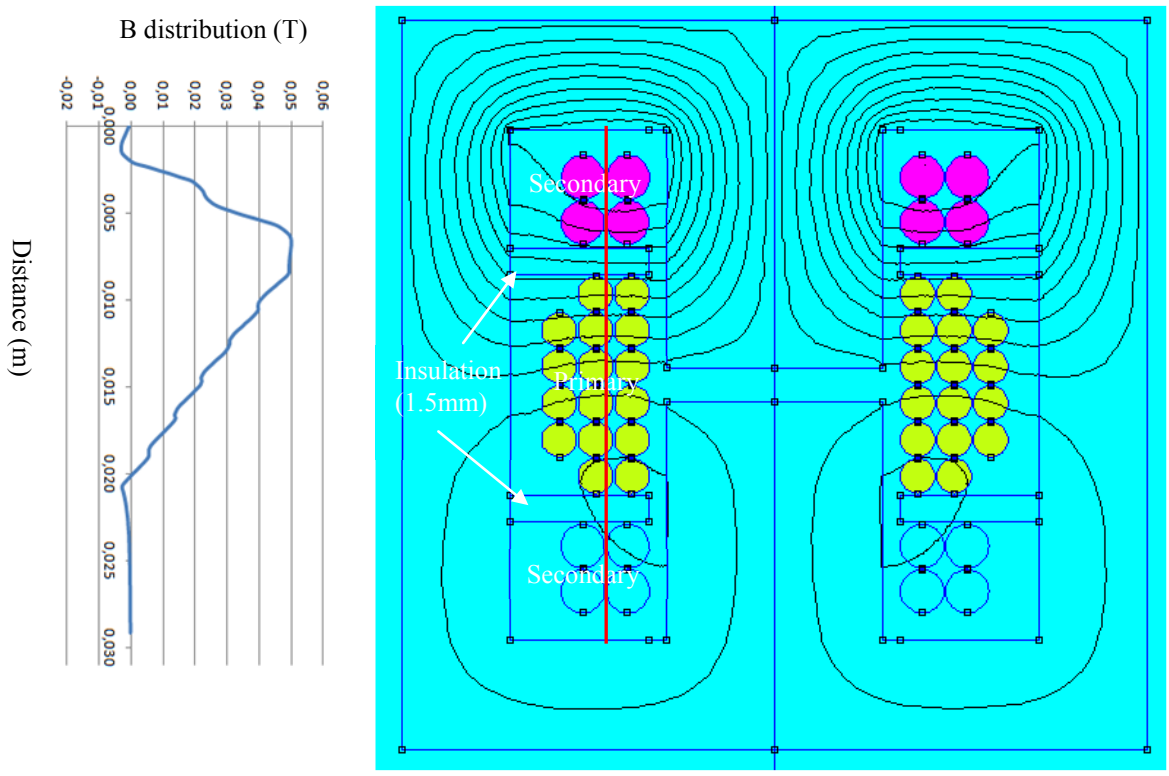


Figure R-12. Réalisation du transformateur avec inductance de fuite l*f*=1.5 µH

Dans cette configuration, une plus forte densité de flux existe dans l'intervalle entre enroulements : Bpk≈50mT. Avec un espace suffisant entre primaire et secondaires, ce transformateur peut ainsi réaliser une inductance de fuite l_f=1.5µH. L'inductance de résonance nécessaire étant plus élevée, il est nécessaire de rajouter un noyau RM12 à entrefer avec 6 tours. La photo d'un prototype de transformateur est donnée à la figure R-13.

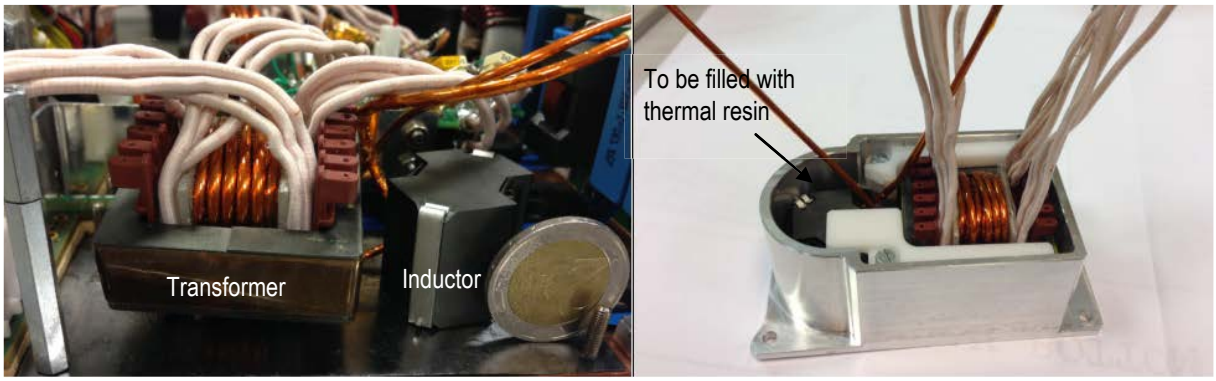


Figure R-13. Transformateur et inductance additionnelle nus (à gauche) et dans un récipient (« sarcophage ») de refroidissement (à droite)

Du fil de Litz (800x0.05mm primaire, 1200x0.05mm secondaire) est utilisé pour éviter l'effet de peau et de réduire l'effet de proximité dans les enroulements du transformateur. Les pertes dans les fils de Litz doivent être finement analysées pour êtres estimées avec précision.
Pour le fil de Litz, le diamètre de chaque brin doit être inférieur à l'épaisseur de peau σ. Sous cette condition, la répartition de courant peut être considérée comme homogène dans la section de chaque brin. Cependant, des pertes importantes peuvent encore être dues à l'effet de proximité. Il est possible de distinguer l'effet de proximité interne et l'effet de proximité externe. L'effet de proximité interne fixe la distribution de courant dans un brin en fonction du courant dans tous les autres brins lorsqu'il n'y a pas de champ externe. L'effet de proximité externe est dû à un champ magnétique externe provenant par exemple, comme dans notre cas, de l'entrefer d'un transformateur. Les pertes dues à l'effet de proximité externe, les principales dans notre cas, peuvent être estimées par l'équation suivante :

$$P_{eddy} = \frac{4\omega^2 l B_{pk}^2 d^2 S}{128\rho}$$

ρ est la résistivité du fil, *d* est le diamètre de chaque brin, *l* est la longueur du fil, Bpk est le pic du champ magnétique externe à une pulsation ω. S est la section effective du fil de Litz,

avec $S = N\pi d^2/4$. Il semble évident que la diminution du diamètre des brins et l'augmentation de leur nombre pour conserver une même section effective permettent de réduire les pertes. Cependant, l'isolant nécessaire autour de chaque brin conserve une épaisseur équivalente. C'est ainsi qu'un plus grand nombre de brins plus fins pour une même section utile totale se traduit par une section totale supérieure, donc par un circuit magnétique plus volumineux. En outre, lorsque des brins plus fins sont nécessaires, le coût du fil de Litz augmente. Ainsi, le diamètre du brin doit être soigneusement sélectionné afin de réaliser le meilleur compromis entre rendement, encombrement et coût. Dans ce projet, nous avons choisi le fil de Litz de type 44AWG avec un diamètre de brin de 50 µm (soit environ 1/3 de l'épaisseur de peau).

Certaines spires de l'enroulement primaire sont plus proches de l'entrefer et baignent dans un champ magnétique plus intense. Dans le but de réduire l'effet de proximité externe, il est intéressant d'éloigner les enroulements du noyau central. Afin d'estimer les pertes dans les enroulements du transformateur il est possible de recourir à la simulation numérique. La figure R-14 donne un exemple de calcul.

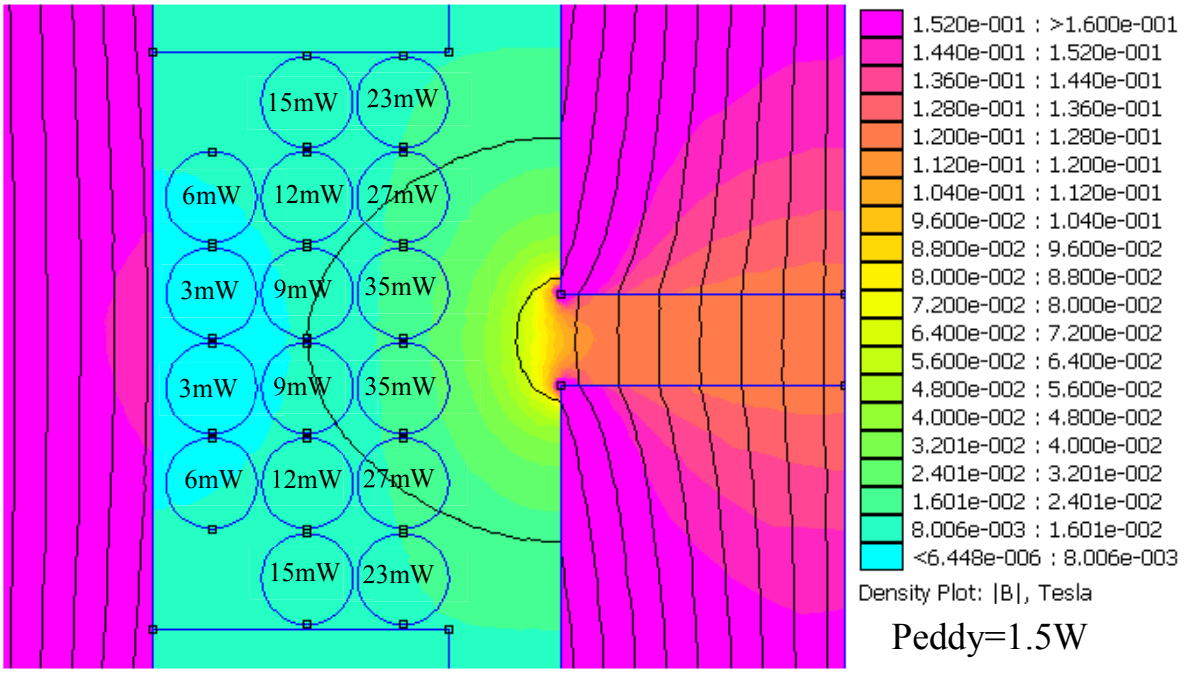


Figure R-14. Calcul des pertes dans chaque spire pour une géométrie donnée

La figure R-14 est relative à une distance de 2,5 mm entre enroulements et noyau central (épaisseur de la « carcasse »). Les pertes totales dans l'enroulement primaire, dues principalement à des courants induits (de Foucault), sont alors de 1.5W. Lorsque la distance diminue jusqu'à 1mm, ces pertes passent de 1.5W à 3.5W.

Dans le cadre de cette thèse, il nous a semblé intéressant de tester un mode de refroidissement innovant. Dans un système de refroidissement à air classique, le profilé d'aluminium n'a pas la capacité d'évacuer efficacement les calories générées par les composants de puissance car des points chauds existent. La solution de refroidissement adoptée ici passe par l'utilisation d'une chambre à vapeur à la base du dissipateur, comme indiqué à la figure R-15.

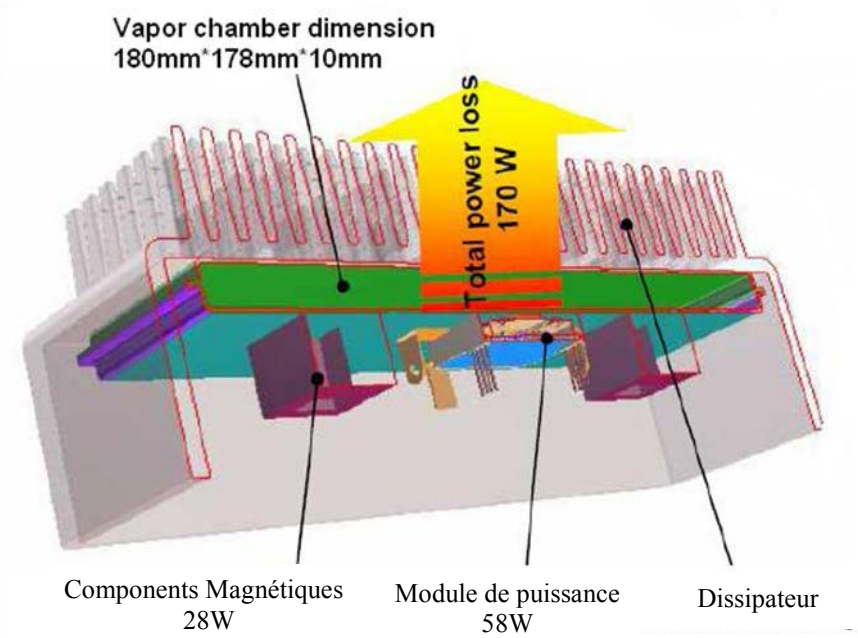
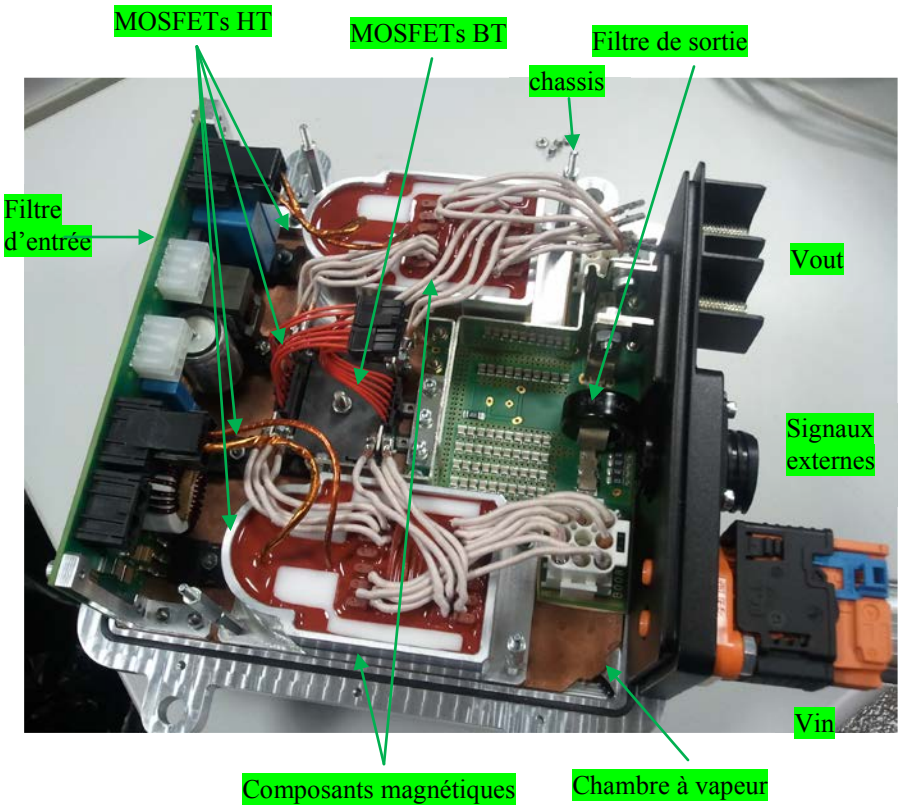


Figure R-15. Utilisation d'une chambre à vapeur à la base du dissipateur

Une chambre à vapeur est un caloduc plat qui utilise le principe de l'évaporation et de la condensation afin de répartir au mieux la chaleur sur le dissipateur, comme une plaque de conductivité thermique très élevée. La chaleur est évacuée par l'intermédiaire d'un fluide qui s'évapore puis se condense assurant ainsi une répartition uniforme de la température et une élimination des points chauds.

Les photos de la figure R-16 montrent l'implantation des composants dans le prototype. Comme les pertes dans le PCB du filtre d'entrée sont limitées, celui-ci est monté verticalement afin de réduire l'encombrement global. Les MOSFETs HT sont placés en dessous du filtre d'entrée et sont fixés directement à la chambre de vapeur par des vis afin de faciliter le refroidissement. Des interfaces thermiques sont toutefois nécessaires pour isoler les MOSFETs HT de la chambre de vapeur. Les composants magnétiques et les modules MOSFET BT sont également montés directement sur la chambre à vapeur. La carte de circuit imprimé de commande est montée sur quatre entretoises, au-dessus des composants de

puissance. Un connecteur externe à 16 broches est utilisé pour échanger des signaux de commande et des signaux de mesure avec l'extérieur. Après assemblage, le prototype a un encombrement global de 2.5l et une masse de 3 kg. Pour une puissance nominale de 2,5kW (puissance crête de 3 kW), cela représente une densité volumique de 1W/cm^3 et une densité massique de 0.83W/kg, ce qui est très important pour ce type de convertisseur. A l'ambiant, seule la convection naturelle est suffisante. Quand la température ambiante s'élevée à 70ºC, une convection forcé avec vitesse du vent 1.5m/s est nécessaire afin de garantir les composants de puissances sont bien au dessous de 105ºC.



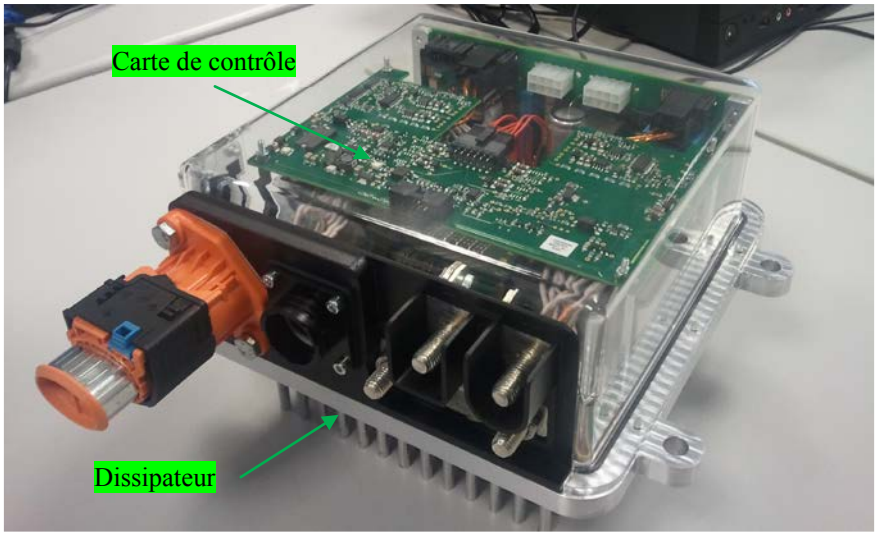


Figure R-16. Prototype du convertisseur LLC réalisé avec une densité de 1W/cm3

Résultats

Les figures R-17 et R-18 montrent les résultats expérimentaux mesurés sur le prototype.

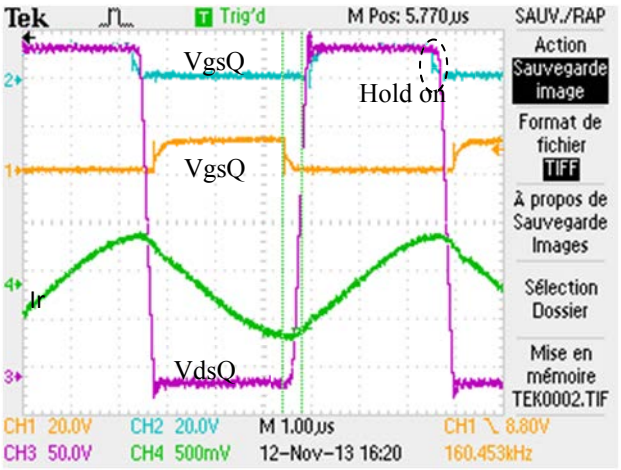


Figure R-17. Formes d'onde au primaire pour la phase B, avec Io = 150A, Vin=350V. (Ir:10A/div)

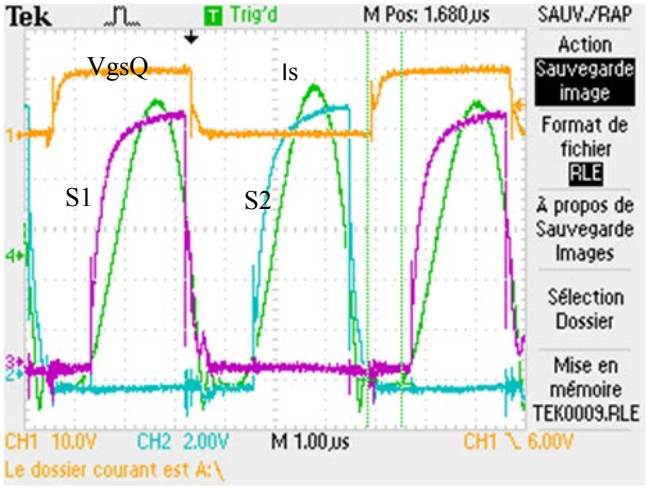


Figure R-18. Formes d'onde au secondaire pour la phase B, avec Io = 150A, Vin=350V. (Is:20A/div)

Les MOSFETs HT choisis (STW88N65M5) sont du type « super-jonction » avec une caractéristique très non-linéaire pour la capacité de sortie : Coss est très élevée à une tension Vds basse. La tension drain-source est maintenue constante au début du blocage ZVS, pendant environ 150 ns, puis la tension décroît linéairement jusqu'à zéro, avant la fin du temps mort. Les MOSFETs sont également mis en conduction en mode ZVS. Le temps mort finalement adopté est de 400ns. La partie secondaire du convertisseur fait appel au

redressement synchrone ce qui mène à des pertes par conduction extrêmement faibles. Comme le montre la figure R-18, le signal de redressement synchrone est pratiquement en phase avec le courant de sortie mais, durant un laps de temps très court, le redressement par transistor n'a pas lieu : le redressement synchrone se termine 300ns avant que le courant ne s'annule. Des pertes par conduction sont prévisibles dans la diode, mais ces pertes sont négligeables compte tenu de son temps de conduction. Le courant de recouvrement inverse (~ 10A) entraîne aussi des pertes de l'ordre de 1.5W par MOSFET. Le rendement a été mesuré pour chaque cellule A et B et pour les deux cellules de puissance fonctionnant ensemble en parallèle (figure R-19).

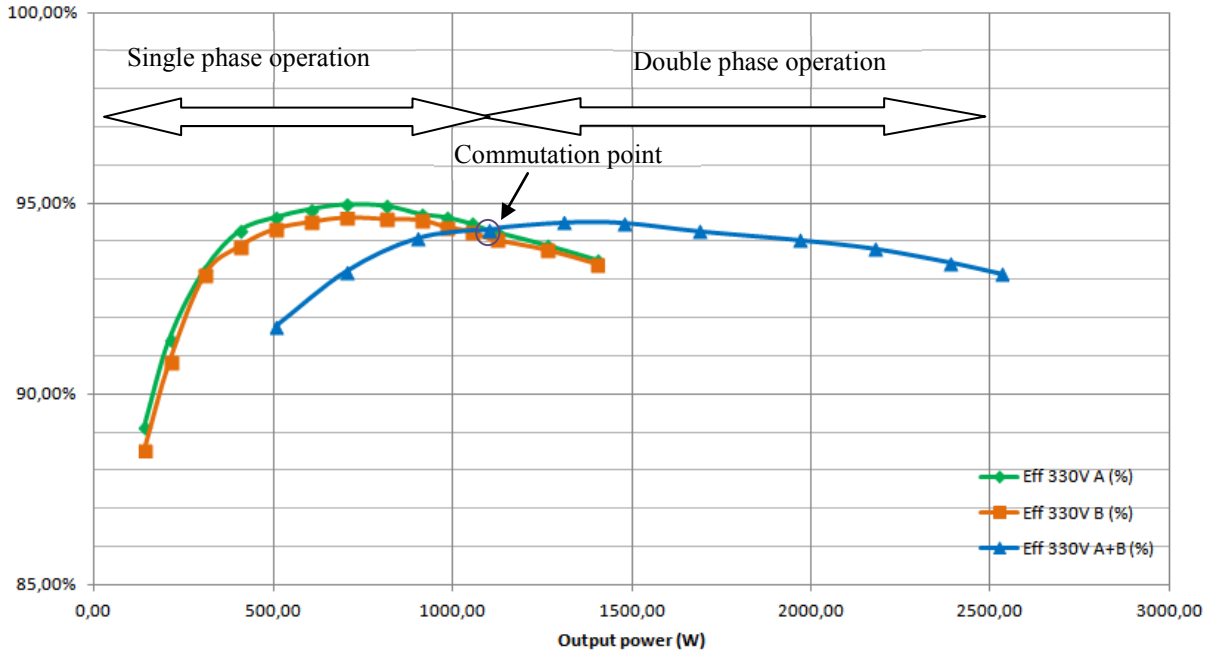


Figure R-19. Rendement mesuré pour Vin = 330V

Le rendement de conversion d'une seule cellule LLC est maximale lorsqu'elle délivre 700 W, avec un rendement maximal de 95% pour la phase A et 94,7 % pour la phase B. En raison des dispersions des composants, les performances de ces deux cellules de puissance sont légèrement différentes. Le rendement commence à diminuer lorsque la puissance de charge dépasse 700W. Il est intéressant de faire fonctionner une seule cellule tant que la puissance appelée par la charge ne dépasse pas 1,1 kW et de faire fonctionner les deux modules simultanément pour une puissance supérieure. C'est ainsi que le rendement de conversion global peut être maximisé. Le rendement continue d'augmenter entre 1,1 kW et 1,5 kW.

Le convertisseur LLC à deux phases permet donc d'obtenir un très bon rendement : η> 94 % de 500W à 2kW ; η > 93 % de 300W à 2,5 kW. Même à très faible charge (140W), le rendement de conversion est d'environ 89 %.

La figure R-20 présente les résultats de mesure CEM du côté haute tension.

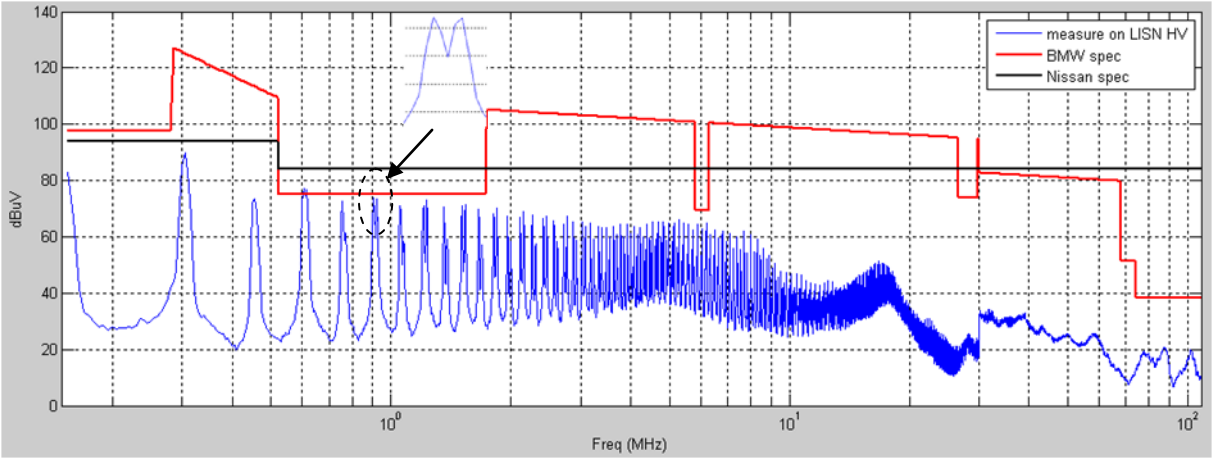


Figure R-20. Mesure CEM de haute fréquence à LISN LV + (détecteur de AVG, Vin = 330V)

Comme le montre la figure R-20, tous les bruits sont maintenus en-dessous des limites spécifiées par des fabricants de véhicules. Le bruit principal est détecté aux fréquences 2k*f*s. L'asymétrie des secondaires de transformateurs (le courant n'est pas parfaitement distribué entre les deux enroulements secondaires du transformateur) provoque des bruits supplémentaires aux fréquences (2k-1)*f*s. En particulier pour *f*s, le niveau de bruit généré est inférieure à celui correspondant à 2*f*s ; cependant, l'atténuation du filtre d'entrée pour *f*s est 15dB plus basse qu'à 2*f*s ; ainsi le bruit mesuré à *f*s devient important devant celui à 2*f*s (72dBμV vs 78dBμV). La symétrie des enroulements secondaires du transformateur doit être précisément contrôlée pour éviter ce bruit.

Pour la composante fondamentale et les premières composantes harmoniques, il n'est pas possible de distinguer une différence entre *f*a et *f*b à cause de la résolution de l'appareil de mesure. À partir de 5*f*s, les différences entre fréquences adjacentes deviennent apparentes. Les niveaux de bruits aux fréquences adjacentes sont égaux, ce qui vérifie que le bruit est superposé dans le domaine fréquentiel. En concevant des filtres d'entrée/sortie basés sur le niveau de bruit généré par une phase, l'autre phase bénéfice naturellement de la même atténuation à une fréquence adjacente.

Dans le convertisseur, l'interaction entre les bruits de commutation de chaque cellule crée des fréquences de battement indésirables, à des fréquences multiples de la différence entre les

fréquences de fonctionnement : un battement à basse fréquence 2(*f*b-*f*a) apparaît en entrée et en sortie. Étant donné que les deux fréquences sont proches l'une de l'autre, ce battement ne peut pas être suffisamment atténué par le filtre passe bas d'entrée ou de sortie.

Pour atténuer ce battement, des condensateurs de découplage avec des capacités suffisantes sont nécessaires à l'entrée de chaque cellule de puissance. De plus, les filtres d'entrée et de sortie ne doivent pas faire apparaitre de résonance à basse fréquence pour éviter d'amplifier ces battements. Ainsi, chaque filtre doit être précisément conçu et contrôlé. Les mesures à basse fréquences sont données à la figure R-21.

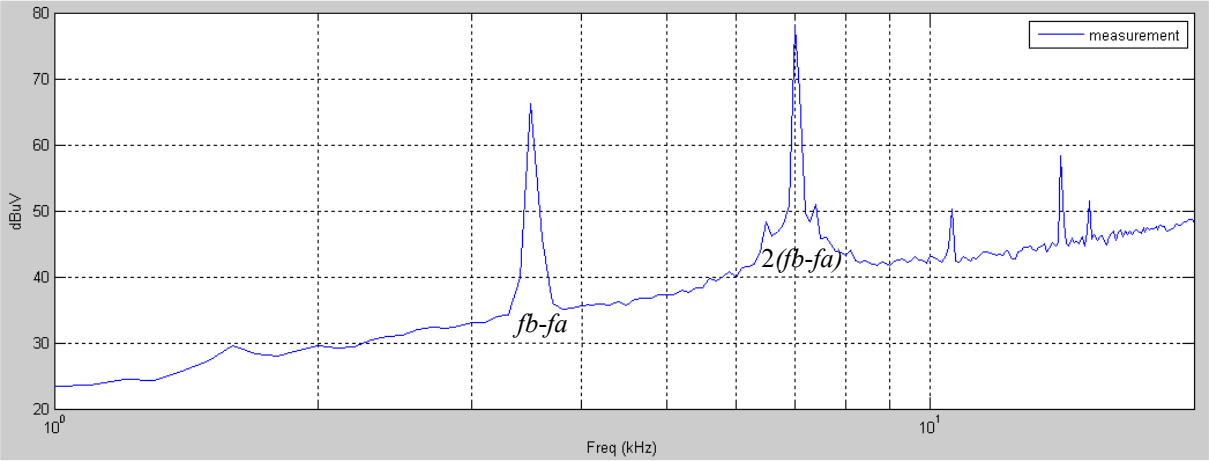


Figure R-21. Mesure CEM de basse fréquence à LISN LV + (détecteur de AVG, Vin = 410V)

Le principal battement à la fréquence 2(*f*b-*f*a) est mesuré à 78dBµV ; un autre battement à la fréquence (*f*b-*f*a) à 65dBµV est dû à l'asymétrie de transformateur. Comme le bruit de battement est inférieur au bruit de commutation principal, il n'a pas d'influence sur le bon fonctionnement du convertisseur LLC et sur ses performances.

Conclusion

La solution consistant à connecter en parallèle deux cellules de puissance LLC est intéressante dans les applications à fort courant, en particulier dans la notre (180A en sortie). Le rendement est ainsi optimisé. Il peut l'être davantage en faisant fonctionner une seule cellule à faible puissance et les deux simultanément à forte puissance. Afin d'équilibrer les courants entre les deux cellules, une stratégie de commande à double boucle est proposée. Elle repose sur des fréquences de fonctionnement indépendantes dans les deux cellules. Les deux fréquences sont légèrement différentes à cause de la dispersion des valeurs de composants dans chaque circuit résonnant.

Outre la conception de cette topologie, ce travail de thèse repose également sur de nombreux essais, à la fois par calcul, par simulation et expérimentalement, dans le but d'améliorer toujours davantage les performances du convertisseur LLC. En particulier, l'utilisation d'un noyau classique en E avec entrefer a été validée pour intégrer toutes les inductances de résonance nécessaires dans le transformateur sous les formes d'inductance de magnétisation et d'inductances de fuite. C'est ainsi que l'encombrement et la masse des composants magnétiques ont pu être minimisés. Le choix même du fil de Litz et celui de son emplacement dans la fenêtre du circuit magnétique ont été optimisés. Les MOSFET BT du secondaire ont été réalisés sous forme d'un seul module IML, ce qui a permis de réduire beaucoup les pertes par conduction ainsi que les résistances thermiques. L'emploi d'une chambre à vapeur a montré son efficacité dans ce type d'application. Le filtrage a lui aussi été optimisé compte tenu d'un petit défaut inhérent au principe retenu : deux fréquences de découpage doivent coexister. Moyennant quelques aménagements, les battements qui en découlent peuvent être rendus négligeables.

En conclusion, le convertisseur LLC à double phase proposé semble être une bonne solution pour construire des convertisseurs de quelques kilowatts à fort rendement et à forte puissance massique. Le prototype réalisé, presque directement industrialisable, convient en particulier pour les applications DC/DC de 2,5 kW HT / BT dans les futurs véhicules électriques et hybrides.

Chapter 1. Introduction

1.1 Backgrounds and project introduction

Power electronics plays an important role in automotive and transport industrial applications, converting normally voltages from 200V to 3000V. Energy saving is now in strong demand to cope with growing demand for electrical applications and limited ecological resources, calling for rapid advancement in power semiconductor devices, conversion, and storage technologies. This puts a considerable pressure on all industries to innovate on levels of systems, device, technology and manufacturing [1-1]. (References are attached at the end of each chapter.)

In Automotive, the upcoming trend for electric vehicles calls for economical, efficient and low cost solutions, based on new packaging and innovative components. By a study combining from Strategy Analytics and IFX it is estimated that in 2015 roughly 6.2 million hybrid and electric vehicles will be produced per year. In total this indicates a market volume of roughly 1 Billion € of automotive power electronics in 2015.

Figure 1-1: Typical electrical vehicles in mass production or demo (PHEV=plug-in hybrid electric vehicle, EREV= extended range electric vehicle, EV=electric vehicule)

Currently a variety of different electric vehicle concepts, battery systems, and individual technical solutions is pursued for concept cars and small fleets of electric vehicles in order to gather experience with this new kind of cars, shown as in Figure 1-1. Technologies are adapted from industry, but the power traction units are far from being optimized with respect to efficiency, volume, or mass production.

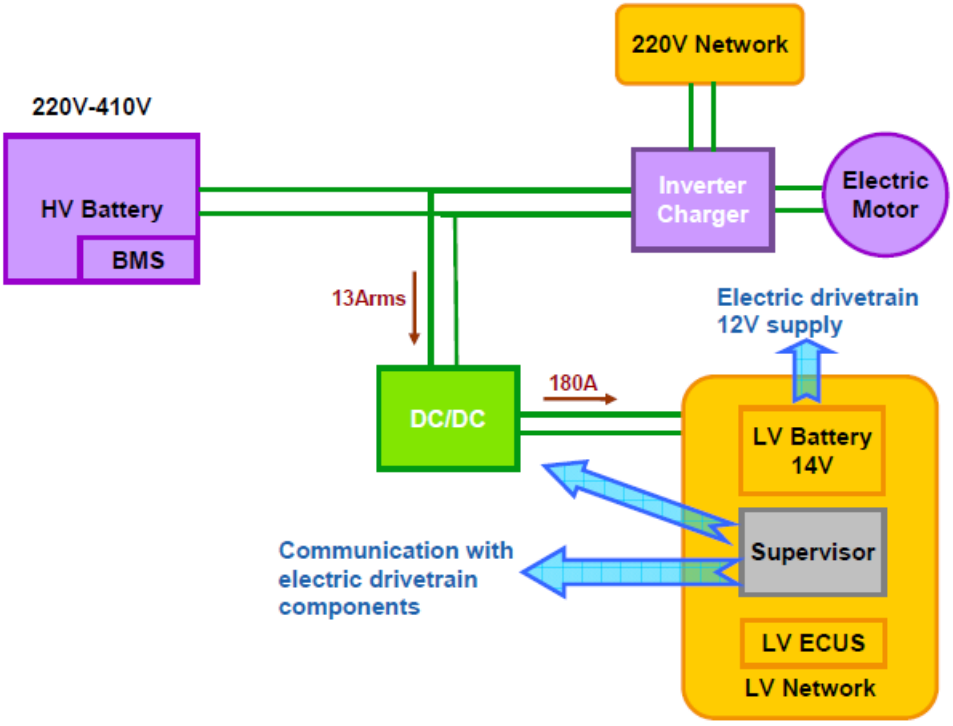


Figure 1-2: A typical mechanical traction and power conversion system in electric vehicles

The traction system in electric vehicles is shown as in the above Figure 1-2. The electric vehicles are principally powered by a high voltage battery permitting to drive the traction chains. The high voltage (HV) battery is constructed by connecting in series or parallel several battery cells, with the number of cells properly selected according to the required power (from 15kW to 100kW depending on the type of vehicle) and the targeted autonomic distance (variant from 100km to 400km depending on the specification). A DC/AC inverter converts the HV battery voltage to three phase AC voltage to drive the electric motors.

Considering the other functions, other equipments are all powered by a classical 14V low voltage (LV) network, as in Figure 1-2. In order to power the LV network, all the electric vehicles are equipped with a HV/LV DCDC converter generating an insulated 14V voltage based on the HV battery. A secondary 14V battery is connected at the LV network for the start, stop and diagnostic phases while the HV battery is not activated during these phases.

The aim of this dissertation is to develop a high efficient DCDC converter, with the following main requirements as electrical parameters:

Table 1-1: Objective specifications of the DCDC converter project

Energy flow	From HV-DC to LV-DC unidirectional
Efficiency	93% peak, >92% from 1kW
Input voltage	220-410V
Output voltage	12-16V
Maxi output power	2.5kW
Mini output power	0W
Maxi continuous output current	180A
Operating temperature	-40ºC to 70ºC by using natural convection
Maximum volume (without heat sink)	2.5L
Mini power density	$1W/cm^3$
Voltage regulation accuracy	±1%

Energy conversion efficiency and power density are the two top concerns for power electronics converters in electrical/hybrid car industries. In order to attain the objectives of conversion efficiency and volume, soft-switching techniques should be adopted to increase the switching frequency and minimize the size of magnetic components and passive filters. Synchronous rectification is mandatory to get high conversion efficiency rather than Schottky diodes. Besides, the converter should also be able to generate the low output voltage based on a large input voltage variation range. Therefore, this dissertation mainly focuses on the topology investigation and performance amelioration to comply with the specified objectives of HV/LV DCDC converters with wide input voltage range operation at a wide output power range.

The converter is designed to be capable of generating 12-16V output. But in order to simplify configuration, the converter demonstrator is regulated to 14V constant output and is connected to a pure resistive power load. This dissertation mainly draws its attention on power electronic issues in circuit operation and efficiency improvement.

1.2 Discussions on existed soft-switching converter solutions

1.2.1 H-bridge phase shift converter

Soft-switching PWM converter, especially H-bridge (full bridge) phase shift PWM converter [1-2], is a widely used topology in HV/LV DCDC conversion, with its typical circuit schematic given at Figure 1-3. Primary side is in full bridge structure and secondary side is in a center-tapped structure.

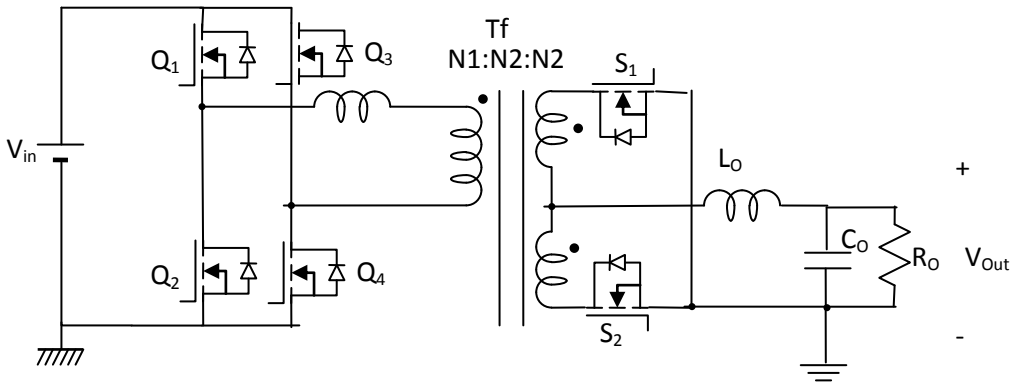


Figure 1-3. The H-bridge phase shift PWM converter

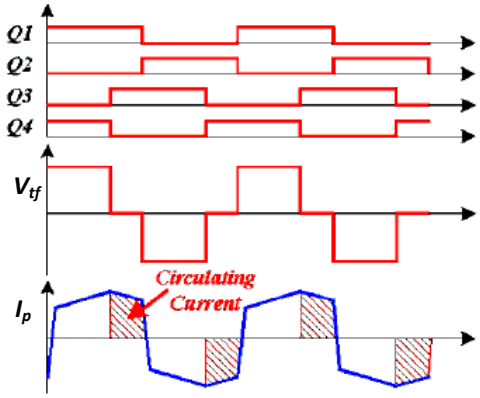


Figure 1-4. Typical waveforms of H-bridge phase shift PWM converter

The phase shift PWM converter operates at a constant frequency, varying the phase shift between the two half bridges to regulate the output voltage. With this topology, it is possible to assure a ZVS soft-switching at the primary MOSFETs and a reduced switching loss can be attained. However, secondary LV MOSFETs are still exposed to hard-switching which influences its efficiency. The recovery current introduces high voltage spikes at the switch-off of MOSFETs due to the secondary leakage inductance and filtering inductor. In this case, a bulky snubber is necessary to limit the voltage spike. MOSFETs with higher drain-source

withstand voltage should be selected, resulting in an increase of the on resistance and conduction loss. This is a common disadvantage of the center-tapped topology with a filtering inductance at output. Another problem, as shown Figure 1-4, large circulating current exists at the freewheeling periods, which greatly deteriorates its efficiency, especially for low input voltage case.

VALEO has designed a first prototype at year 2011 using full bridge phase-shift topology based on the same specifications as Table 1-1, shown as in the Figure 1-5.

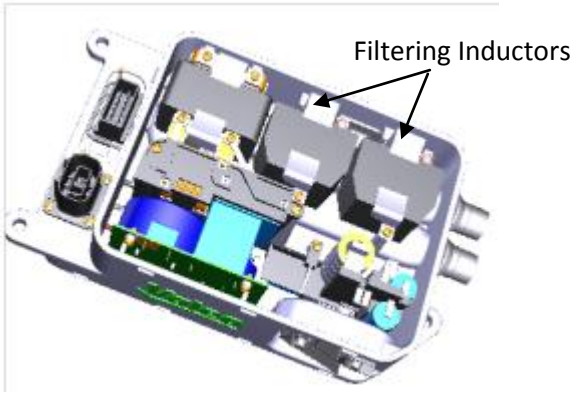


Figure 1-5. VALEO's 2.5kW, 400/14V, 100kHz, full bridge phase shift DCDC converter with 0.61W/cm^3 power density

H bridge phase-shift topology with synchronous rectification is applied. As shown in Figure 1-5, two bulky filtering inductors (each with L*f*/2) occupy too much volume due to high conductive current thus the total power density is deteriorated. Due to the hard switching-off of LV MOSFETs, the switching frequency is limited to 100kHz, which restricts the volume miniaturization of magnetic components. In all, the converter prototype performs a peak efficiency of 92%, with a volume 4.8L and a power density of 0.61W/cm3, water-cooled. Referring to Table 1-1, the developed prototype cannot attain the mechanical requirements and the efficiency is not in line with the new market expectations.

1.2.2 Series resonant converter

The most efficient way to get a high power density is to increase the switching frequency so that the size of magnetic components can be greatly reduced. Resonant converters are possible to work at higher switching frequency thanks to very low switching loss. In resonant

converters, the output/input voltage conversion ratio is varied by its switching frequency, other than varying its pulse width or phase shift.

Half-bridge series resonant converter [1-3, 1-4, 1-5, 1-6] is a popular topology in resonant converters for HV/LV power conversion. The resonant tank is composed by a resonant inductor Lr, a resonant capacitor Cr and a transformer Tf, shown as in Figure 1-6. The voltage conversion ratio equation of the resonant tank is expressed as follows:

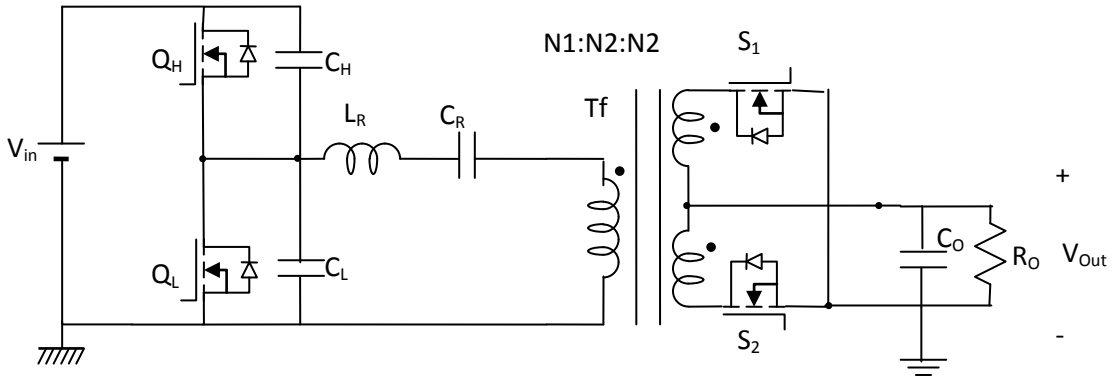


Figure 1-6. Half bridge series resonant converter with synchronous rectification

$$G = \frac{1}{1 + j\frac{\pi^2}{8} Q\left[\frac{f_s}{f_r} - \frac{f_r}{f_s}\right]} \quad (1\text{-}1)$$

Where f_r is the resonant frequency; $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, f_s is the switching frequency; Q is the quality factor, $Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} = \frac{Z_c}{R_{ac}}$; Rac is the equivalent load transferred to the primary side, $R_{ac} = R_{out}\frac{8}{n^2\pi^2}$. The overall conversion ratio of the converter should also consider the half bridge (1/2) and the transformer turns ratio (N_2/N_1) .

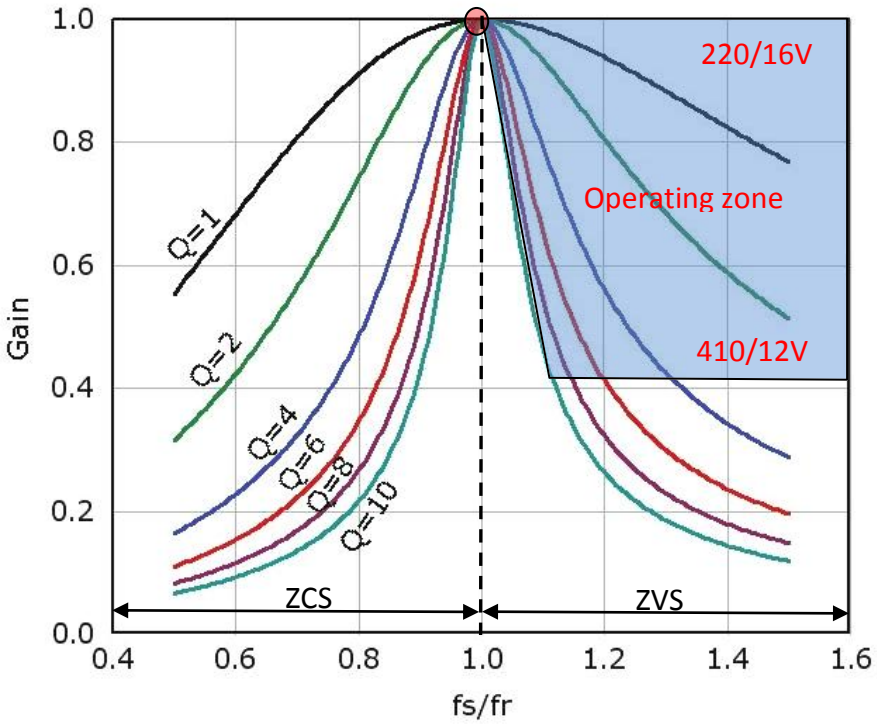


Figure 1-7. Voltage conversion ratio characteristics of series resonant converter

The resonant tank and the load constitute a voltage divider thus the DC voltage transfer ratio is always ≤1. At the resonant frequency, the impedance of tank is 0 so the DC gain is maximal. At this point, the DC gain is independent with the load thus it is called the load independent point. As to HV MOSFETs operating at high efficiency, the operation at ZVS (where gain slope is negative) is highly preferred than ZCS (where gain slope is positive) thus the switching frequency is always kept higher than the resonant frequency.

Series resonant converter brings many advantages over H bridge phase shift converter. As the transformer's secondary side behaves as a current source to the load, thus only a filtering capacitor is sufficient. Furthermore, the reverse-recovery current of LV MOSFETs does not introduce a voltage spike and the MOSFETs can be switched on at ZVS and switched off totally at ZCS.

The main problem of series resonant converter is its degraded performance at light load & high input voltage conditions. Referring to Figure 1-7, for the curve Q=1(10% load), the switching frequency increases with the increase of input voltage and finally the frequency will be very high if input voltage is increased to 410V; skin effect and proximity effect became significant and the efficiency at low load is deteriorated. As to no-load conditions, the resonant circuit is in series with an open circuit thus the resonant operation is no longer

possible. Based on the above analysis, the series resonant converter attains a high efficiency at nominal power while its efficiency at light load condition is sacrificed, thus it is not a good solution for the targeted converter.

1.2.3 Parallel resonant converter

Parallel resonant converter [1-7, 1-8, 1-9] is also a well-known converter. Its circuit schematic is shown as follows:

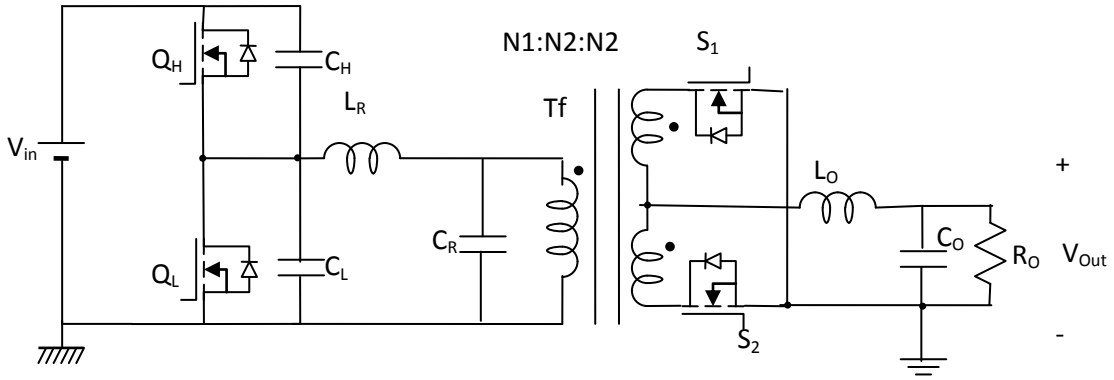
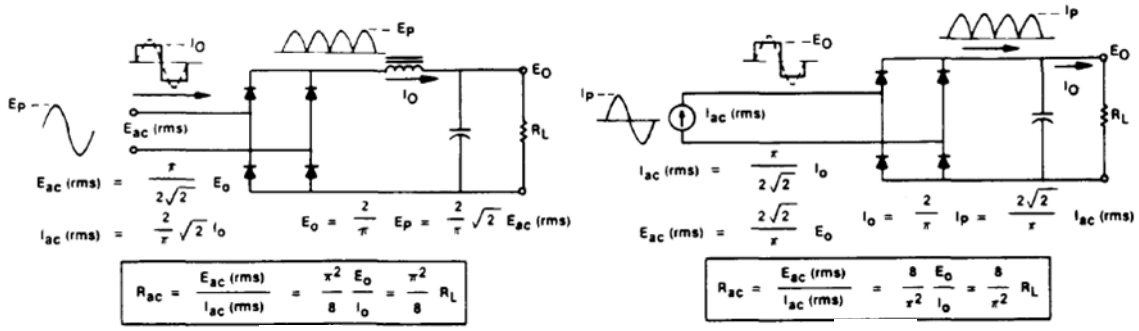


Figure 1-8. Half bridge parallel resonant converter with synchronous rectification

The voltage conversion ratio equation of the parallel resonant tank is expressed as follows:

$$G = \frac{\pi^2}{8} \frac{1}{\frac{\pi^2}{8}\left[1-\left(\frac{f_s}{f_r}\right)^2\right] + j\frac{f_s}{f_r}\frac{1}{Q}} \quad (1\text{-}2)$$

The difference between series resonant and parallel resonant converter is that the resonant capacitor behaves a voltage source to the secondary side; this voltage needs to be further filtered by a LC filter at the output. The equivalent resistance calculations of a current source resonant converter (series or LLC in 1.2.5) and a voltage source resonant converter (parallel or series-parallel in 1.2.4) are shown as follows [1-10]:



(a) (b)

Figure 1-9. Equivalent ac resistors presented by different rectifier loads: (a) voltage source converter, (b) current source converter

Following the above figure, the definitions in parallel converters are:

$$R_{ac}=\frac{\frac{V_{out}}{n}*\frac{\pi}{2}}{nI_{out}*\frac{4}{\pi}}=R_{out}\frac{\pi^2}{n^2 8},\ Q=\frac{R_{ac}}{\sqrt{L_r/C_r}}=\frac{R_{ac}}{Z_c}.$$

The maximum gain is obtained at the resonant frequency with $G_{\max}=\frac{\pi^2}{8}Q$. The voltage conversion ratio characteristics and the operation region are shown in the following figure:

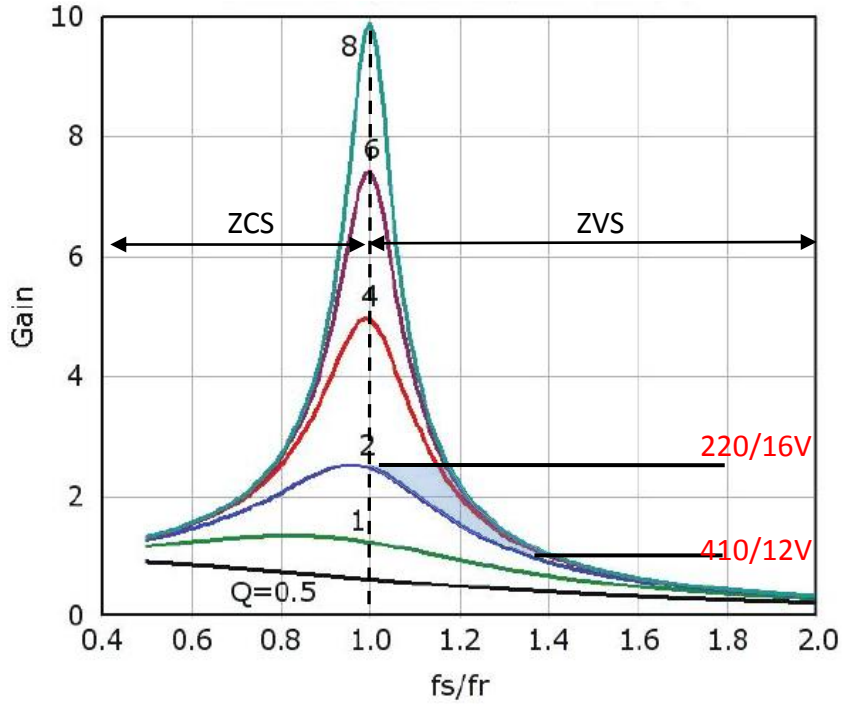


Figure 1-10. Voltage conversion ratio characteristics of parallel resonant converter

The operating region of parallel resonant converter is much smaller than series resonant converter. The switching frequency does not change too much to keep the output voltage regulated. Thus the light load problem and no load incapability do not exist in parallel resonant converters.

One drawback of parallel resonant converter is its high reactive power. Even at light load, the resonant cell exhibits small impedance and the resonant current is high. Another drawback of parallel resonant converter is that it behaves as voltage source to the secondary side, thus a filtering inductor Lo is mandatory. As a result, this topology sees all the drawbacks of center-tapped transformer with filtering inductor discussed in 1.2.1. In conclusion, the parallel resonant converter is not a good candidate.

1.2.4 Series-parallel resonant converter

The schematic of series-parallel resonant converter [1-11] is shown at the following Figure.

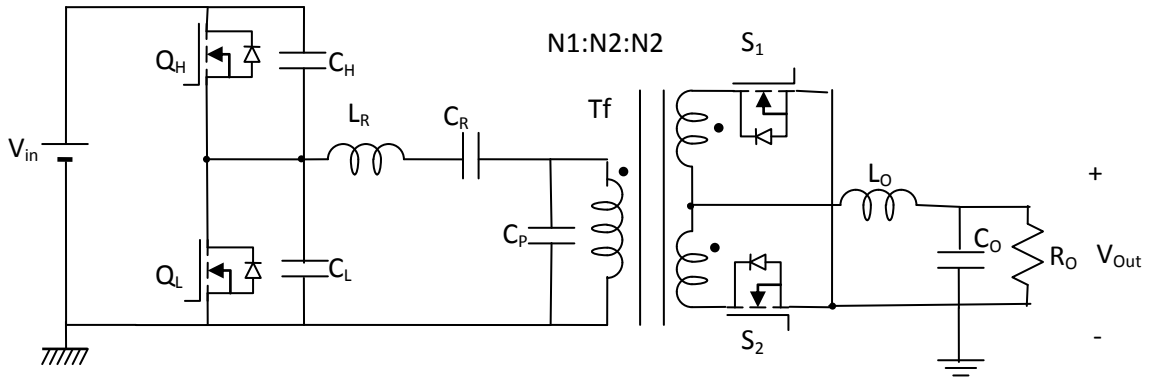


Figure 1-11. Half bridge series-parallel resonant converter with synchronous rectification

The resonant tank is composed by three components: resonant inductor Lr, series resonant capacitor Cr, parallel resonant capacitor Cp. The resonant tank can be considered as a combination of the series resonant tank and the parallel resonant tank, thus it benefits both the advantages of two converters. The voltage conversion characteristics are shown at the following figure:

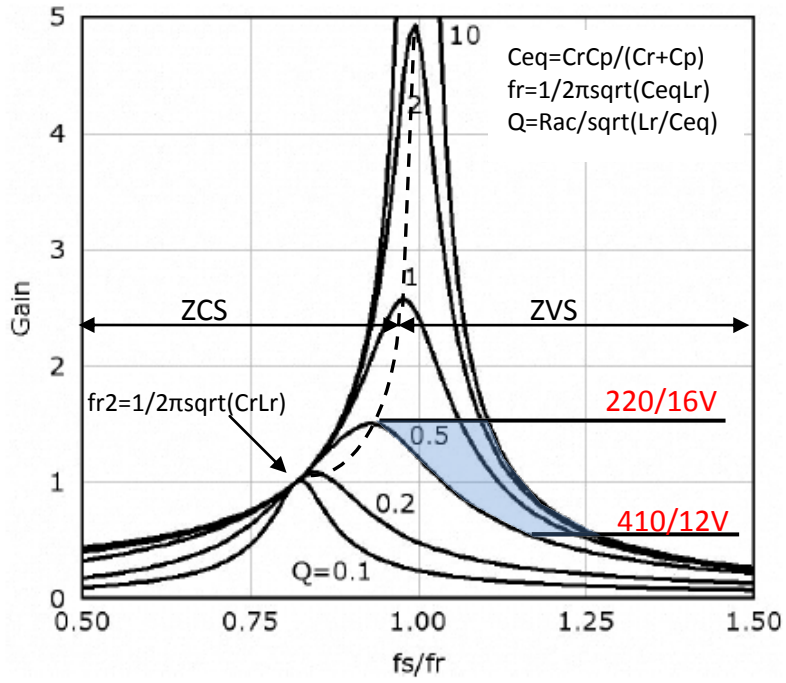


Figure 1-12. Gain characteristics of series-parallel resonant converter (Cr=Cp)

As shown in Figure 1-12, the series-parallel resonant converter has two resonant frequencies. At the series resonant frequency f_{r2}, the impedance of the Lr and Cr is 0 and the voltage conversion ratio is 1, like the series converter. At the main resonant frequency f_r, the gain increases sharply, like the parallel converter. The operation region is shadowed at the above figure. We can see that the series-parallel converter has a narrow switching frequency range and no-load regulation capability. At light load conditions, due to the presence of a capacitor Cp, the reactive power is much smaller than that of the parallel resonant converter.

Unfortunately, like the parallel converter, the series-parallel converter also needs a filtering inductance at the output side. Therefore, it still sees all the inconveniences of center-tapped transformer with filtering inductor discussed in 1.2.1. Thus in conclusion, the series-parallel resonant converter is not a good candidate.

1.2.5 LLC resonant converter

The simplified circuit schematic of LLC [1-12, 1-13] is shown in the following figure:

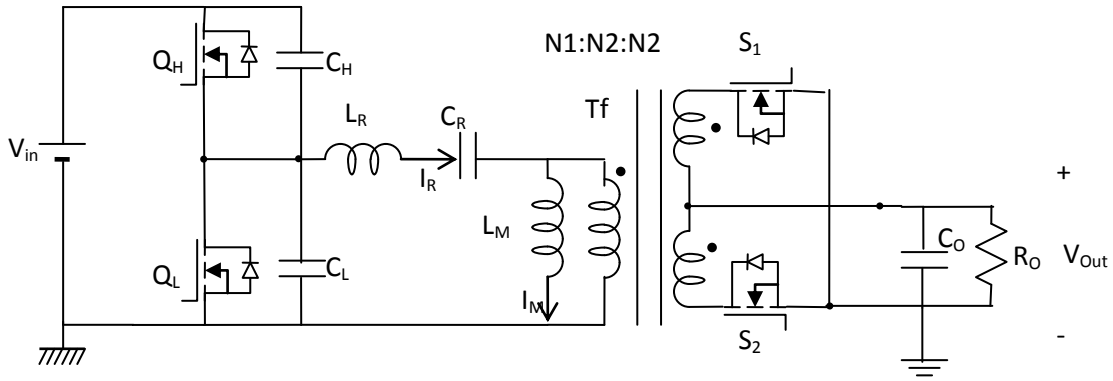


Figure 1-13. Half bridge LLC converter with synchronous rectification

Same as the series resonant converter, the center-tapped transformer in LLC disposes a current source to the load thus no bulky inductor is needed. The resonant tank contains two inductors, one resonant capacitor and a transformer. The inductor Lm can be integrated into the transformer as its magnetizing inductance. Furthermore, the resonant inductor can be fully or partially integrated into the transformer's leakage inductance. The overall volume of magnetic components can be minimized; this is a great advantage of LLC converter over other converter types.

The operation of LLC converter can be divided into three modes: (1) ZCS mode, (2) ZVS discontinuous current mode and (3) ZVS continuous current mode, as shown as in the following figure:

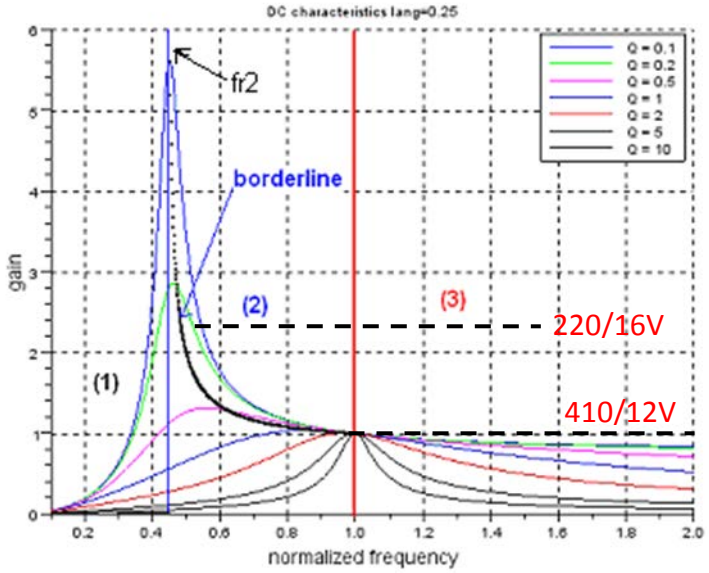


Figure 1-14. Gain characteristics of LLC resonant converter (Lm=4Lr)

As discussed above, the ZCS mode should be avoided. Both mode (2) and mode (3) exhibit ZVS operation. The key waveforms of LLC in the mode (2) and mode (3) are shown as follows (The detailed discussions of these three operating modes will be presented at the Chapter 2).

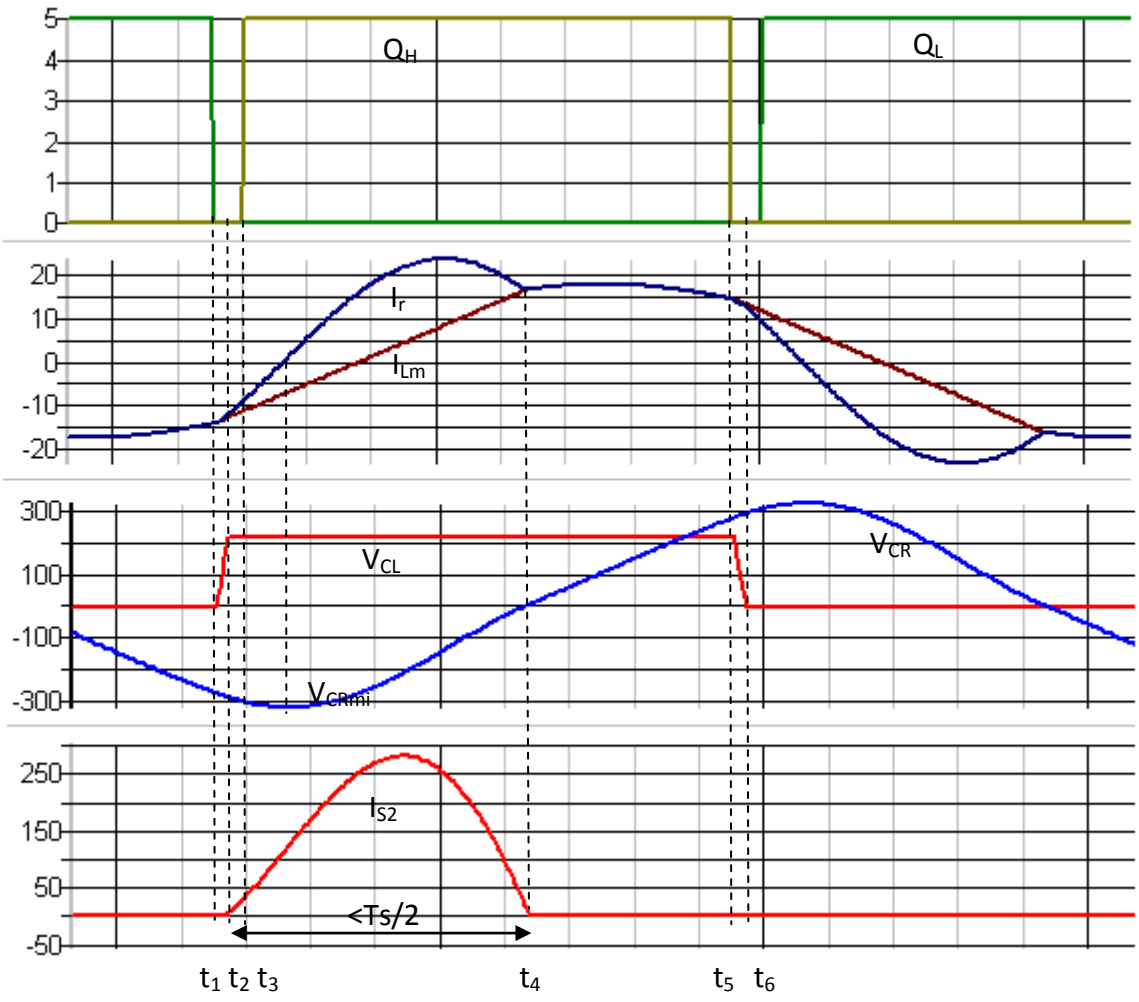


Figure 1-15. Operating waveforms of LLC converter at ZVS-DCM

The operation of LLC converter in ZVS-DCM can be divided into the following different stages:

a. [t_1-t_2]: ZVS turn off

When Q_L is switched off, capacitor C_L starts to be charged and C_H starts to be discharged by the resonant current. The presence of the ZVS capacitor C_L makes the voltage across Q_L increase linearly thus results in a ZVS switch-off. It is also required that the charging time of

ZVS capacitor should be shorter than the dead time, thus the C_L can be fully charged to Vin and C_H be discharged to 0 within the dead time.

B. [t_2-t_3]: ZVS turn on

After C_H has been fully discharged to zero, the body diode of Q_H conducts to maintain the current continuity of Ir and the voltage across Q_H is zero. The Q_H then can be switched on at ZVS at the instant of t_3.

C. [t_3-t_4]: Lr resonant with Cr

In this period, the transformer's voltage VLm is clamped by the load to a constant value equal to Vout/n. The resonant inductor Lr is then in resonance with the capacitor Cr and the magnetizing current increases linearly from negative to positive, which signifies that the Lm shifts from energy releasing to energy charging between t_3 and t_4.

D. [t_4-t_5]: Lr resonant with Cr and Lm

This period starts from the moment that the resonant current Ir meets the magnetizing current ILm. No current circulates at the transformer's secondary side and the Lm participates into resonance, thus the resonant period is expended and the current remains nearly constant at this period. As no current are sent to the secondary side, the current at the secondary MOSFET remains at zero and this is the so-called discontinuous current mode.

E. [t_5-t_6] : ZVS switching

This period is the same as the period [t_1-t_3] except that the operation order of MOSFETs is totally reversed. The Q_H is switched off in ZVS mode and the Q_L will be switched on in ZVS mode.

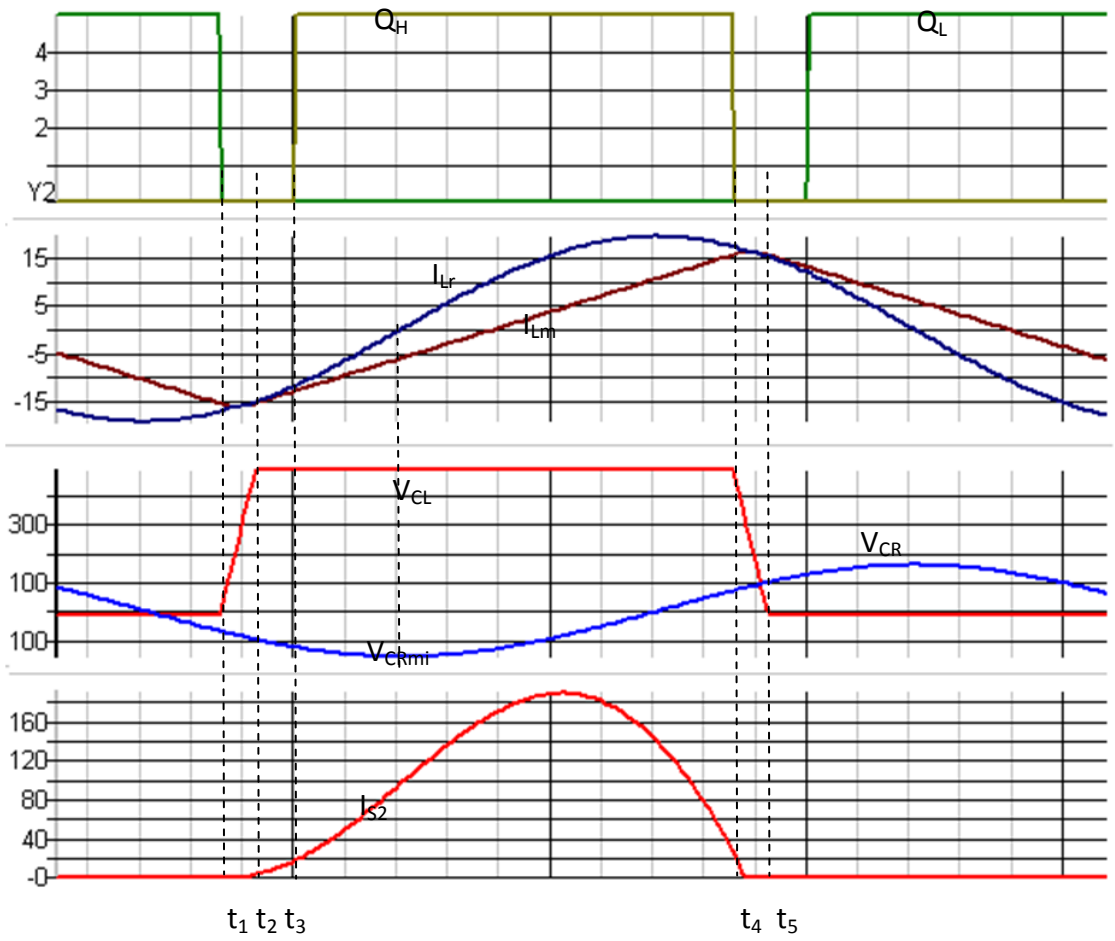


Figure 1-16. The operation of LLC resonant converter in ZVS-CCM

The difference between ZVS-CCM and ZVS-DCM is that stage [t_3-t_4] in CCM lasts until the end of the switching period. The secondary pulse current duration equals to the half switching period, which is called the continuous current mode. As switching period is lower than the resonant period, the transformer is never liberated from being clamped.

LLC converter overcomes all the inconveniences of other converter topologies, provides design flexibility and both step-down and step-up functions. It has to paid attention that in LLC, the reverse-recovery current may cause a voltage spike due to transformer winding's wire parasite inductance, but this voltage spike is highly limited compared to that of parallel or series-parallel converter. Furthermore, ZVS capability from no load to full load makes the LLC converter one of the most desirable topologies in energy conversion. The following figure presents a developed LLC mock-up from Virginia Polytechnic University [1-14, 1-15]:

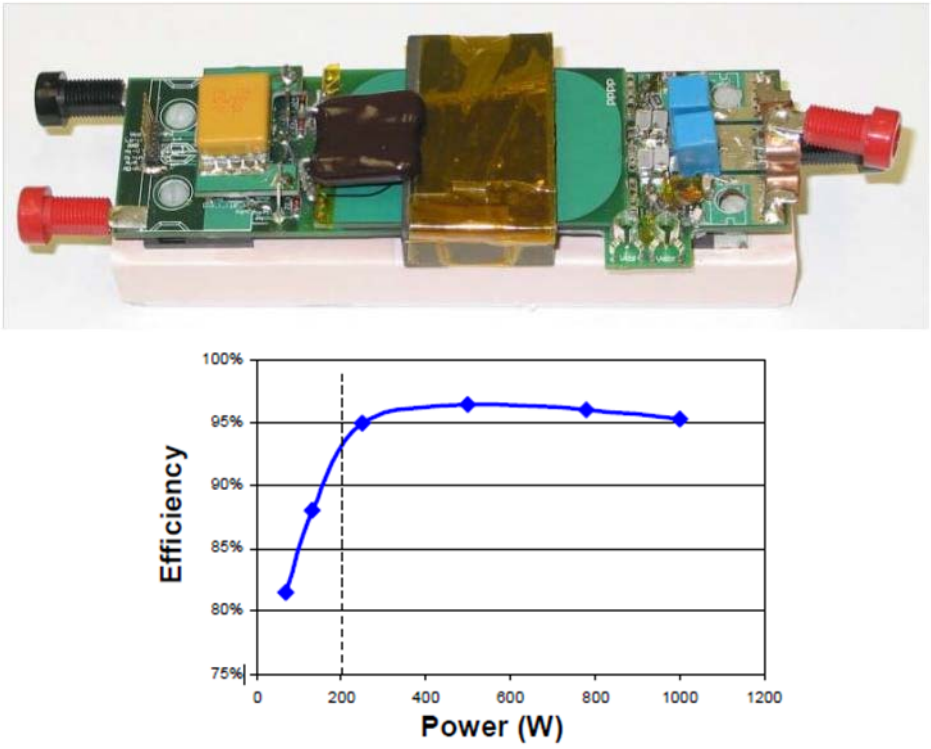


Figure 1-17. 1MHz 1kW, 400V/48V converter mock-up of Virginia Polytechnic University, peak efficiency up to 96%, with 8.9W/cm^3 power density (only main components)

As reported at the above figure, only one magnetic component is adopted to include all the magnetic components. No filtering inductor appears at the output side and the efficiency goes up to 96%. In all, considering the aspects of volume minimization and efficiency improvement, LLC topology is a more competent candidate than other topologies for energy conversion.

1.3 Challenges of LLC resonant converters

Although LLC converter has aroused much popularity in designing high efficient DCDC converters, the following issues need to be further improved.

1.3.1 High efficiency among large load range

In electric/hybrid vehicles, the targeted 2.5kW automobile DC/DC converter may operate at any power from 0 to 2.5kW, but the estimated operation time is different at different power ranges, shown as in the following figure:

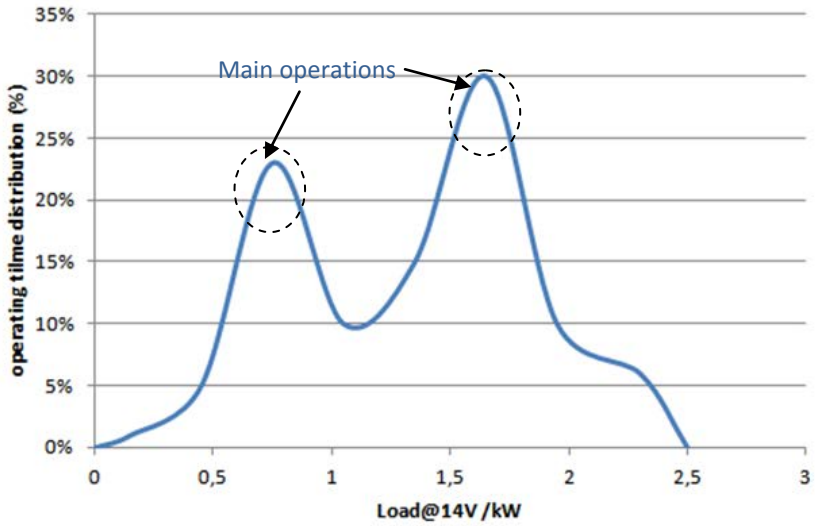


Figure 1-18. Example of operating time distribution of the targeted 2.5kW converter

As shown in the above figure, the converter has higher probabilities in operating mainly at two power ranges: 600-900W and 1.5-1.8kW. Assuring high conversion efficiency at these above two power ranges is very important to improve the overall performance of the converter in energy savings. Like all the other types of converters, traditional LLC converter is able to perform high conversion efficiency at the nominal load but efficiency is deteriorated when load decreases (referring to Figure 1-17). It is thus important to find a solution to keep a high efficiency at a large load variation range, especially at the two power ranges mentioned above.

1.3.2 High output current arrangement

One critical difficulty in this project is how to arrange secondary high output current efficiently. As the output voltage is very low, the converter should deliver up to 180A DC current. The traditional solution to tackle with high conduction current is to parallel more semiconductor components. The problem of this solution lies in the aspects of equal current sharing among the paralleled MOSFETs [1-16, 1-17]. For the static current, MOSFETs in parallel is a current divider where overall current is shared between MOSFETs according to their R_{dson}; for the dynamic current, the important parameter is the threshold voltage (Vgsth) since the MOSFET with lowest Vgsth switches on as the first one and off as the last one, thus conducts higher current during transients.

As a result, due to a slight difference on R_{dson} and Vgsth between MOSFETs in parallel, power loss cannot be distributed equally. Paralleling several MOSFETs to reduce the

conductive power loss is not a good solution. Some other new topologies as power cell interleaving permitting to arrange high output current should be studied and investigated.

1.3.3 Large voltage variation capability at limited frequency range

Various EMC requirements in electric vehicles authorize a high level of switching noises at [280 530] kHz, shown as in the following figure as an example:

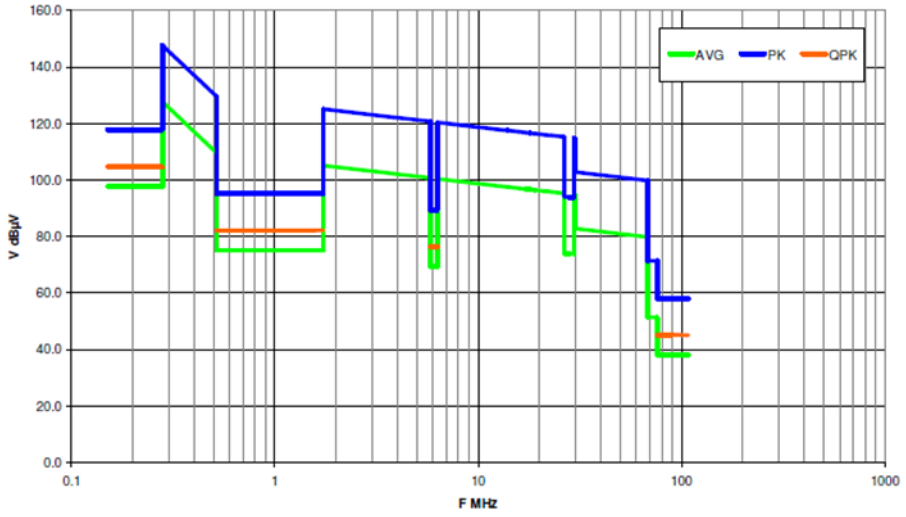


Figure 1-18. EMC specification for HV battery defined by car constructors BMW

To limit the main noise frequency into the described noise range, the switching frequency can be set between [150, 250] kHz (noise frequency can be doubled in LLC). If LLC converter is designed to fully compromise the input voltage variation range, a high gain should be attained at the minimum frequency, and this gain should be precisely calculated and controlled. Based on the established first-harmonic model, the voltage conversion ratio can be calculated precisely and the whole calculation process is described in this dissertation.

Following this proposed process for LLC circuit dimensioning, one can design a LLC converter, based on the required input and output voltage ranges, to obtain the resonant cell parameters under limited switching frequency range. However, when input voltage variation is large, a low Lm is always derived following the calculation process. Too low Lm results in a high circulating current and a bad power factor, which influences its efficiency. As a result, how to broaden the input voltage range while keeping a high power factor (high efficiency) is an essential topic to be solved in this dissertation.

1.3.4 Transformer improvement and integration

Transformer is a key part in LLC resonant converters while its dimension greatly influences the final volume of the prototype. Thanks to higher switching frequency 150-250kHz, the transformer can be selected with a low effective core area. A successful transformer design in LLC converter should include its magnetizing inductance and resonant inductance within the transformer to minimize the total volume of magnetic components. Planar cores are highly preferred in power electronics converter design due to its limited height, large dissipation area and printed PCB board as windings. The following figure shows several transformers in Planar E cores and ER cores.

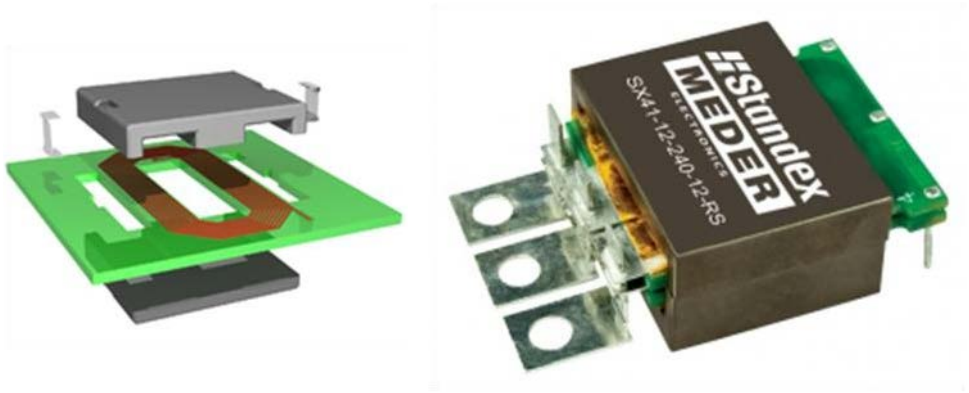


Figure 1-19. Planar E cores and Standex center-tapped transformer with Planar ER cores

Planar core offers convenience in the aspects of package simplicity and thermal conductivity. However, as high power LLC converter adopts usually a very low magnetizing inductance, large air-gap should be integrated into magnetic cores. Planar cores have limited height to include a large air-gap. Furthermore, to integrate the resonant inductance as leakage inductance, planar cores have insufficient window to separate the primary and secondary windings, making it less flexible to design sufficient leakage energy storage. Other core types which can integrate a large air-gap and high leakage energy should be investigated to replace the planar core.

At higher switching frequencies, Litz wire is often adopted as winding solution rather than copper foils or printed PCB to avoid the skin effect and proximity effect. Large air-gap creates large eddy-current loss at Litz wire, especially to those close to air-gaps; this loss should be precisely quantified and the winding method should be improved to reduce this loss.

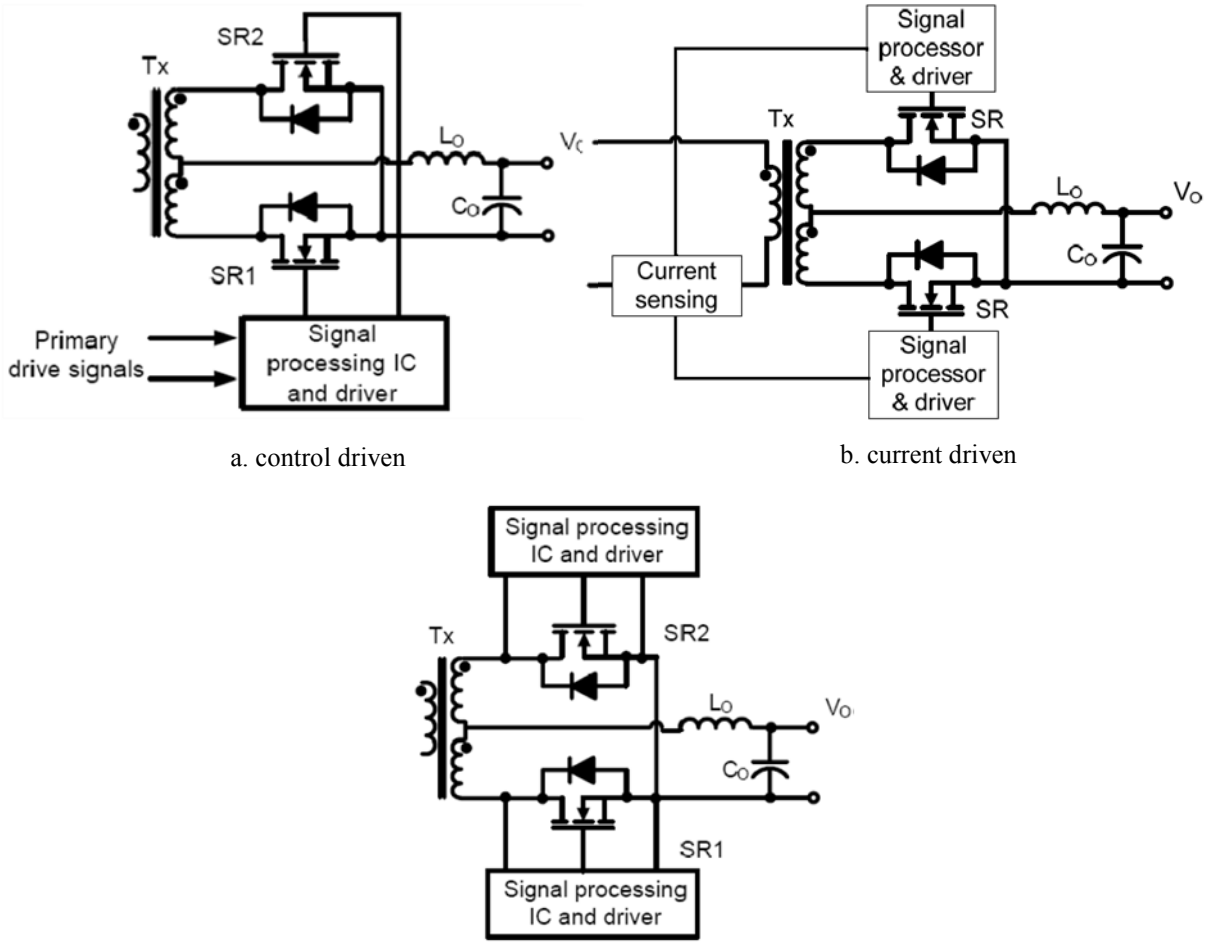
1.3.5 Component and system for effective cooling

High output current generates higher power loss at secondary MOSFETs than primary MOSFETs. Discrete semiconductor components are difficult to be cooled effectively due to its package thermal resistance. Designing and investigating a dedicated power module is a preferred solution to replace the discrete semiconductors.

As dissipated power and power density increase, new enhanced and reliable cooling solutions are needed, other than liquid loop with pump, micro channel, etc. Two phase systems (Heat Pipe, Loop Heat Pipe (LHP)) have proven their reliability and heat transfer capability in spatial applications for decades. They can now be adapted to ground applications and offer improved heat transfer and integration capabilities, in particular vapor chambers with heat pipes.

1.3.6 Robust synchronous rectification

Synchronous rectification (SR) can be classified by its control type into three categories: control driven SR, current driven SR and voltage driven SR.



a. control driven

b. current driven

c. voltage driven

Figure 1-20. Three types of synchronous rectification circuit

In CCM PWM converters, secondary MOSFETs conduction time is in phase with primary control, the control driven SR can be applied. But in LLC converter, the secondary current is not in phase with primary control except for operating at load independent point. Apparently, the control driven SR is not a good solution for LLC converter. Current driven SR uses a current transformer to sense the current information. As in LLC converter, the sensed primary current is the sum of the magnetizing current and the transformer current thus current control SR is neither a good candidate for LLC. The only solution for LLC converter is the voltage driven SR: the drain-source voltage of MOSFETs is sensed and processed to determine the on and off timing of MOSFETs.

However, the sensed drain-source voltage in voltage driven SR suffers from external interferences and internal parasites, reducing its robustness. It is difficult to control the measurement precision in ~mV level. A non precise measurement causes either an early

switch-off or a late switch-off of MOSFET, which reduces the overall efficiency and may cause catastrophic operation failure. A more robust system for SR should be investigated and applied in LLC converter.

1.4 Dissertation outline

Chapter 2 proposes to use double phase parallel-parallel interleaved LLC to share the total high output current. The efficiency performance of single cell and double cell LLC is compared. A power cell switching logic is introduced to assure a high efficiency at large load variation range. As to the resonant tank parameters dimensioning, the equivalent circuit based on first-harmonic model is established and the characteristics of LLC are discussed. A new circuit design procedure is proposed in this dissertation: the influence of leakage inductance is considered and the magnetizing inductance should be carefully adjusted. This part also gives the design considerations for ZVS condition fulfillment.

Chapter 3 is dedicated to the operation and control of the double-phase LLC converter. Problems of traditional phase-shift parallel LLC is investigated here and a new control method for equal current sharing is described in this paper. The LLC's ac signal model is analyzed by Simplis modeling software and the regulators design for control loops are described in this chapter. Also, some other protection circuits, as soft-start, over current protection, over voltage protection, are presented in this chapter.

Chapter 4 is dedicated to the performance and system improvement of designed LLC converter. To cope with high secondary conduction loss at LV MOSFETs, an inserted molded lead-frame module integrating all MOSFETs dies is developed. Several transformer realization proposals are investigated and compared in this chapter, including material selection, resonant inductance integration, and eddy current loss analysis. Synchronous rectification is described and a new robust SR scheme is proposed to get improved phase compensation results. An air cooling system based on vapor chamber is designed in this prototype, with thermal experimental results verifying the performance of this cooling solution. Finally, the main performance results are reported in this chapter.

In Chapter 5, the EMC issues, mainly conducted DM noise issues of proposed double phase LLC converter are presented. The EMI noise emission characteristics of proposed double phase LLC are discussed and the phenomenon of low frequency beating is analyzed in detail. Input and output filter are designed for noise attenuation. The EMC performance of this designed prototype is validated through experimental results.

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Chapter 2. Parallel-parallel double phase LLC: Topology and Dimensioning

2.1 From single cell LLC to double cell LLC

2.1.1 Challenges of single phase LLC resonant converters for high current output

For HV/LV power conversion, LLC resonant converter generally keeps a very competitive efficiency in designing DC/DC power supplies in low or medium power level [2-1 – 2-5]. Generally, the reported LLC resonant converters in literatures are under 1.5kW, especially between 300W and 1kW [2-6 – 2-8]. Increasing load brings the following two main difficulties:

The first difficulty of increasing the LLC converter's power level lies in the transformer core realization. Table 2.1 shows the dimensioning results of a 2.5kW LLC converter and 1.25kW LLC converter with the same specified input voltage and output voltage. In terms of dimensioning the resonant tank parameters for a 2.5kW LLC converter, as shown in Table 2.1, the required transformer's magnetizing inductance is 12μH, with a transfer ratio N_1/N_2=16. Even if the secondary turn number is set to N_2=1, an inductance factor of A_L=50nH is still needed for realizing the low magnetizing inductance, which is too low to be realized practically. For example, as to a transformer core with an effective area A_e=200mm^2 (B_{pk}≈150mT at 150kHz), the required air-gap length is about 6mm. Currently, no commercial magnetic cores are available in the market with such a huge air gap. Furthermore, huge air gap enables more fringing flux penetrating the windings and causes additional winding losses due to eddy current. Special gapping technologies should be applied to the magnetic cores to integrate large air-gap; for example, two or more air gaps should be created, which increases the design and production complexity. However, as to a 1.25kW LLC converter (power is half reduced), the required transformer's magnetizing inductance is doubled, shown as in Table 2.1. The inductance factor is then increased to A_L=100nH, thus a more rational air-gap length is obtained. A centralized air-gap with e≈3mm is sufficient for creating the required inductance factor and many magnetic cores are available at the market, such as E41/21/15, E41/21/20, E42/33/20, etc.

Table 2-1. Parameter dimensioning comparison results for 2.5kW and 1.25kW LLC resonant converters, Vin=220-410V, Vout=14V

Parameters calculated for	2.5kW cell	1.25kW cell
Resonant inductance (Lr)	3.75µH	7.5µH
Resonant capacitance Cr (nF)	100nF	50nF
Magnetizing inductance Lm (µH)	12µH	24µH
RMS resonant current (I_{r_rms})	36A	18A
RMS current per switch, HV side (I_{Q_rms})	25.2A	12.6A
RMS current per switch, LV side (I_{S_rms})	160A	80A
Primary MOSFET STW88N65M5 (Rdson=29mΩ)	2 per switch	1 per switch
Secondary MOSFET IPB180N06S4-H1 (Rdson=1.5mΩ)	2 per switch	1 per switch
Transformer windings	Pri. 1600 strands of 44AWG Sec. 2400 strands of 44AWG	Pri.800 strands of 44AWG Sec. 1200 strands of 44AWG

The second difficulty is that higher power increases sharply the conduction losses at the semiconductor devices and transformers. As shown in Table 2.1, the RMS current at the primary and secondary MOSFETs in 2.5kW LLC is two times higher than that in a 1.25kW LLC. In order to lower the overall conduction loss, two MOSFETs should be paralleled at both HV switch and LV switch. The number of strands in transformer's windings should also be increased thus it results in a larger transformer volume, which makes it even more difficult for obtaining a low magnetizing inductance.

In all, increasing LLC converter's power level creates difficulties in transformer realization and increases the primary resonant current and secondary pulse current. New topologies or ways of interleaving should be proposed to better treat these problems.

2.1.2 Proposition of double phase LLC resonant converter and its operational strategy

Considering the difficulties in building a 2.5kW LLC converter compared to a 1.25kW LLC converter, paralleling two power cells of 1.25kW is an efficient way to achieve high power conversion efficiency without paralleling more MOSFETs or increasing transformer's wire

gauge. Figure 2-1 is the framework of the proposed double phase LLC resonant converter by paralleling two LLC cells.

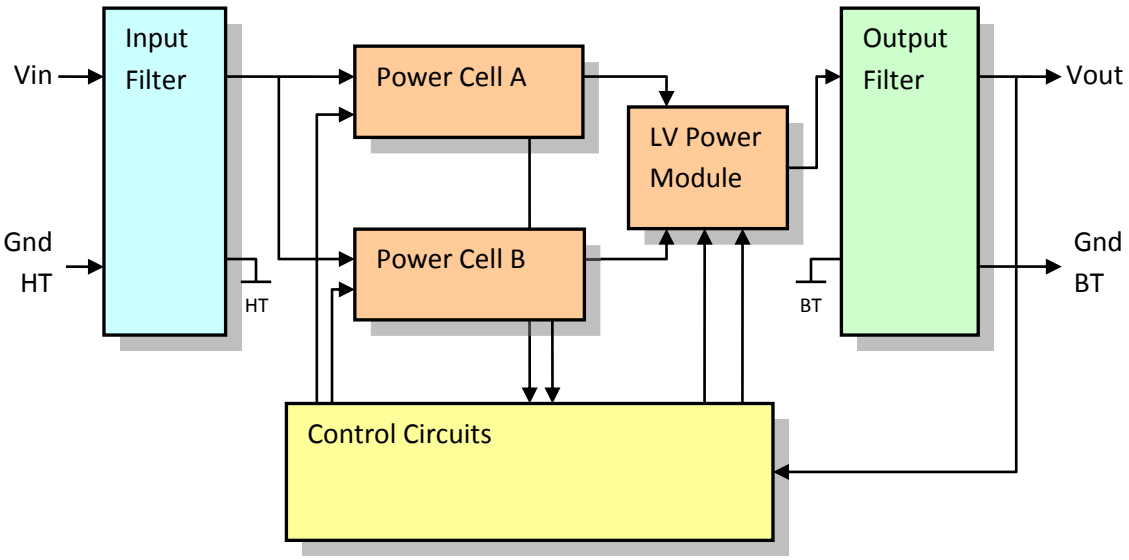


Figure 2-1. The framework of proposed double phase LLC resonant converter

As shown in Figure 2-1, both the two power cells A and B share the same input filter and the same output filter. Each power cell contains its own power MOSFETS in half-bridge topology, resonant capacitors, resonant inductors and transformers. The transformer's secondary windings are connected to a power module which contains four LV MOSFETs (2 for power cell A, 2 for power cell B). All the LV MOSFETs are integrated into the power module mounted on the cold plate to get a better cooling effect. The control circuit contains the regulators, MOSFETs drivers, auxiliary power supplies and synchronous rectification controllers, etc. Power sharing between the two cells shall be balanced to better distribute the current among different power units. An innovative solution will be proposed to achieve this good power sharing and is described in Chapter 3. The primary circulating current and secondary pulse current can be greatly reduced and the current constraints imposed to the HV/LV MOSFETs will be decreased and balanced among different power units. The proposed operational principles of the double cell LLC resonant converter is shown as follows:

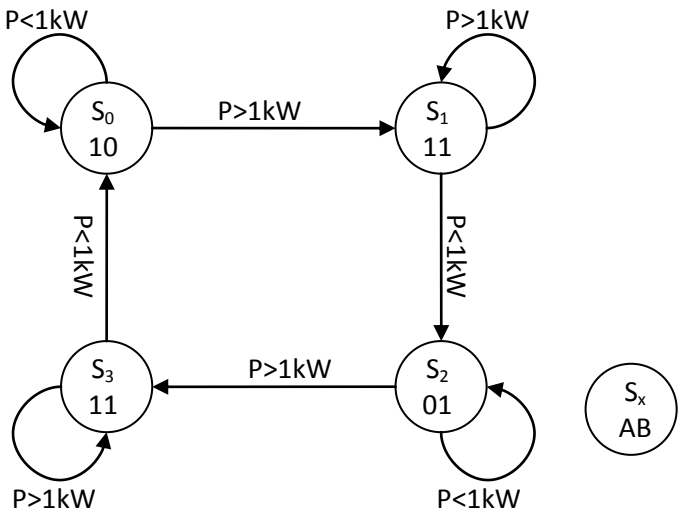


Figure 2-2. State diagram of cell switching

The operating strategy is as follows: When the converter is started at light load, power cell A operates to supply current to the load, this corresponds with the state S_0. When output power is higher than 1kW, the power cell B is switched on and both the two power cells supply current to the load, with each power cell shares 50% of the output power, which corresponds to the state S_1. Then when load is again reduced to lower than 1kW, the power cell B remains on and the power cell A is off, while the state is moved to S_2. The optimal switch-point is pre-set to be 1kW, but shall be checked and adjusted following experimental results to get an overall optimized efficiency. Thus through this cell switching strategy, both the two power cells operate simultaneously only if necessary (at heavy load). As each power cell's operating time is almost the same at a long term, this control strategy also assures an equal aging speed of the two resonant cells and extends greatly the converter's operating life. Furthermore, when one power cell fails to operate, this converter is also possible to work with the other power cell.

In order to make a predictive comparison on power losses existed in single phase and the proposed double phase LLC converters, especially conduction loss and drive loss, simulations are executed using the configurations shown as in Table 1-1 and power loss results are reported at the following Figure 2-3 and Figure 2-4. The Figure 2-5 shows the efficiency prediction comparison between single phase LLC and double phase LLC, by considering only the conduction losses & drive losses. Switching loss and core loss are temporally not taken into consideration for this analysis.

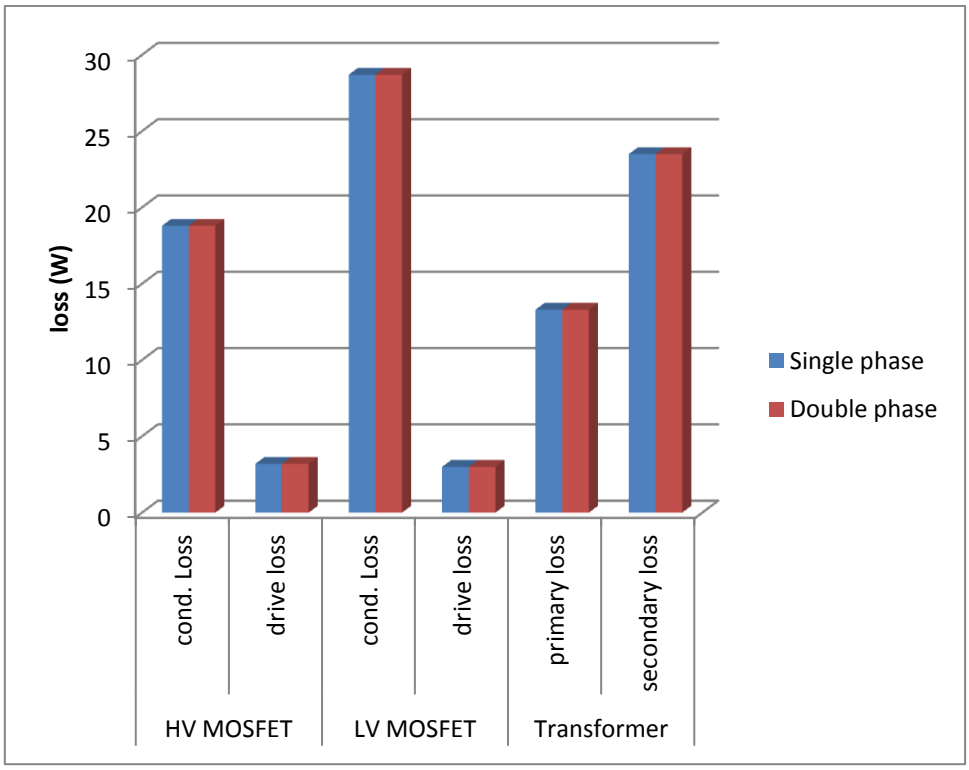


Figure 2-3. Comparison of the calculated power loss between single phase LLC converter and double phase LLC at 2.5kW

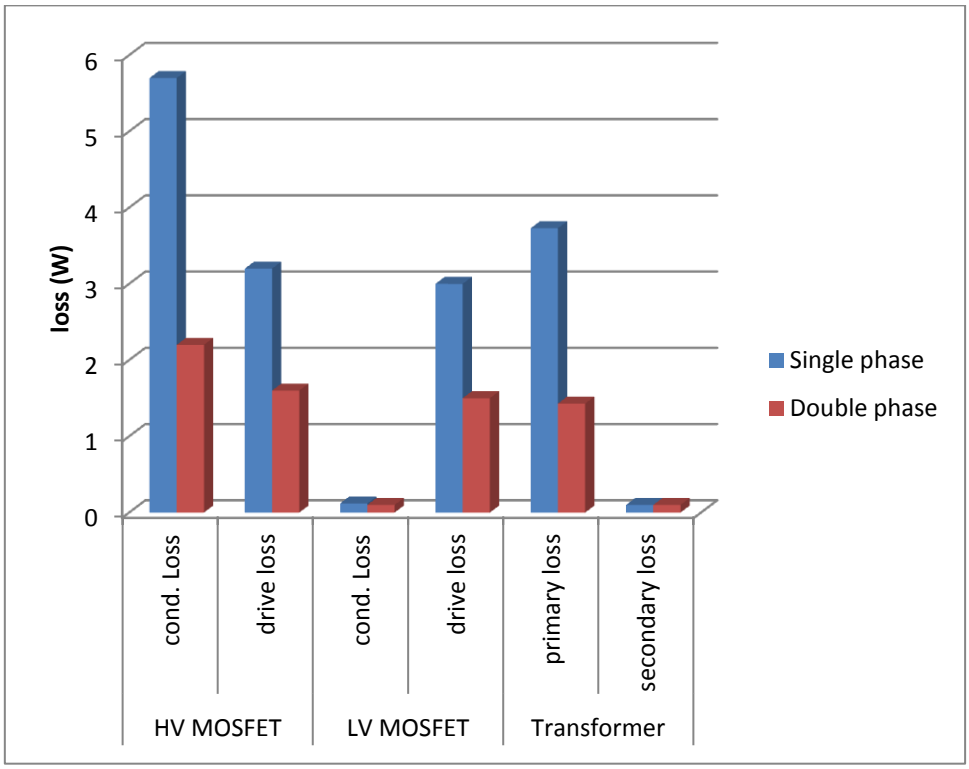


Figure 2-4. Comparison of the calculated power loss between single phase LLC converter and double phase LLC at 100W

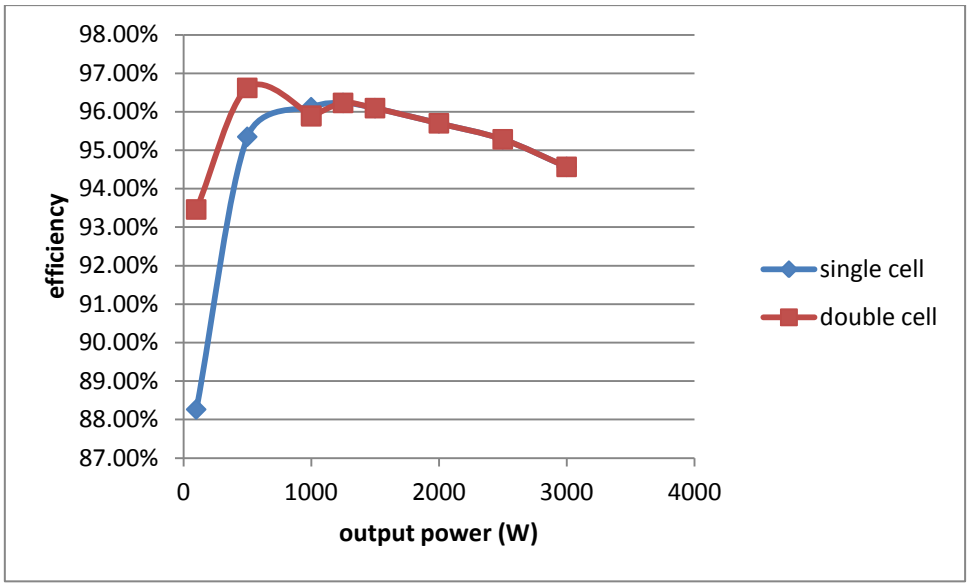


Figure 2-5. Comparison of the calculated power loss between single phase LLC converter and double phase LLC at 100W (considering only conduction losses & drive losses)

At nominal power, assuming that the current is well distributed between the two paralleled MOSFETs, the efficiency of double cell LLC is the same to single cell LLC. From Figure 2-5, the efficiency of these two structures from 1kW to 3kW is equal. However, at light load conditions (Pout<1kW), the performance of double cell LLC converter is more interesting. When load is reduced to lower than 1kW, one power cell is switched-off and only one power cell continues to operate. Other than single cell LLC whose efficiency continues to decrease from 1kW to zero load, the double phase LLC's efficiency is firstly increased until 500W and then start to be decreased. At 100W, the secondary current is very small and the conduction losses at LV MOSFETs and transformer secondary windings for both two structures are very limited. However, a higher circulating current exists at single cell LLC than double cell LLC (16A versus 7.8A due to a lower power factor at light load for single cell LLC than for double cell LLC), which causes higher conduction loss. Referring to the Figure 2-4, the power loss, especially primary conduction loss in double cell converter is greatly reduced. Furthermore, only one cell operates in light load, with only 2 HV MOSFETs and 2 LV MOSFETs switching instead of 4 as for single phase LLC. The MOSFETs drive loss thus can be reduced by 50%.

It is obvious that by applying the double cell structure together with the proposed power cell switching strategy, an overall high efficiency could be obtained at a large output power range from 100W to 3kW. The double cell LLC converter has special interests in improving the power conversion efficiency at light load conditions and obtaining an equal aging speed thus an extended operating life. This is quite interesting since the designed DC/DC converter in electric vehicles has a large probability of operating under 1kW, where in this condition double phase LLC is an excellent candidate in designing automobile DCDC converters.

2.2 LLC optimal dimensioning

As two power cells with each cell at nominal power of 1.25kW is needed for building the double phase converter, this part concerns the dimensioning of a 1.25kW LLC power cell. How to optimize the design procedures to get a wide input/output voltage variation, while keeping a limited operational frequency range is detailed in this part.

Various dimensioning methods are proposed to determine and optimize the resonant cell parameters to improve its performance. Paper [2-9] has proposed a design work flow-chart for LLC power cell dimensioning. In [2-10], the author proposes a calculative approach to determine each parameter step by step. This approach enables the authors to have a rough idea of the resonant circuit. Some design considerations can also be found at [2-11] and [2-12]. But seldom of them includes the effect of leakage inductance into consideration, thus the obtained designing results work well only under several ideal conditions. In [2-13] and [2-14], the author do consider the effect of secondary leakage inductance in increasing voltage conversion ratio, but fails to detect the left-shift phenomena of the converter's load-independent point and the models proposed are not accurate enough. In order to keep a large input voltage variation range at limited frequency range, the magnetizing inductance should not be set too far from Lr. With high switching frequency and high nominal power, secondary leakage inductance has a great influence on the characteristics of LLC power cell and needs to be considered in this design. The proposed design procedures can be explained as in Figure 2-6.

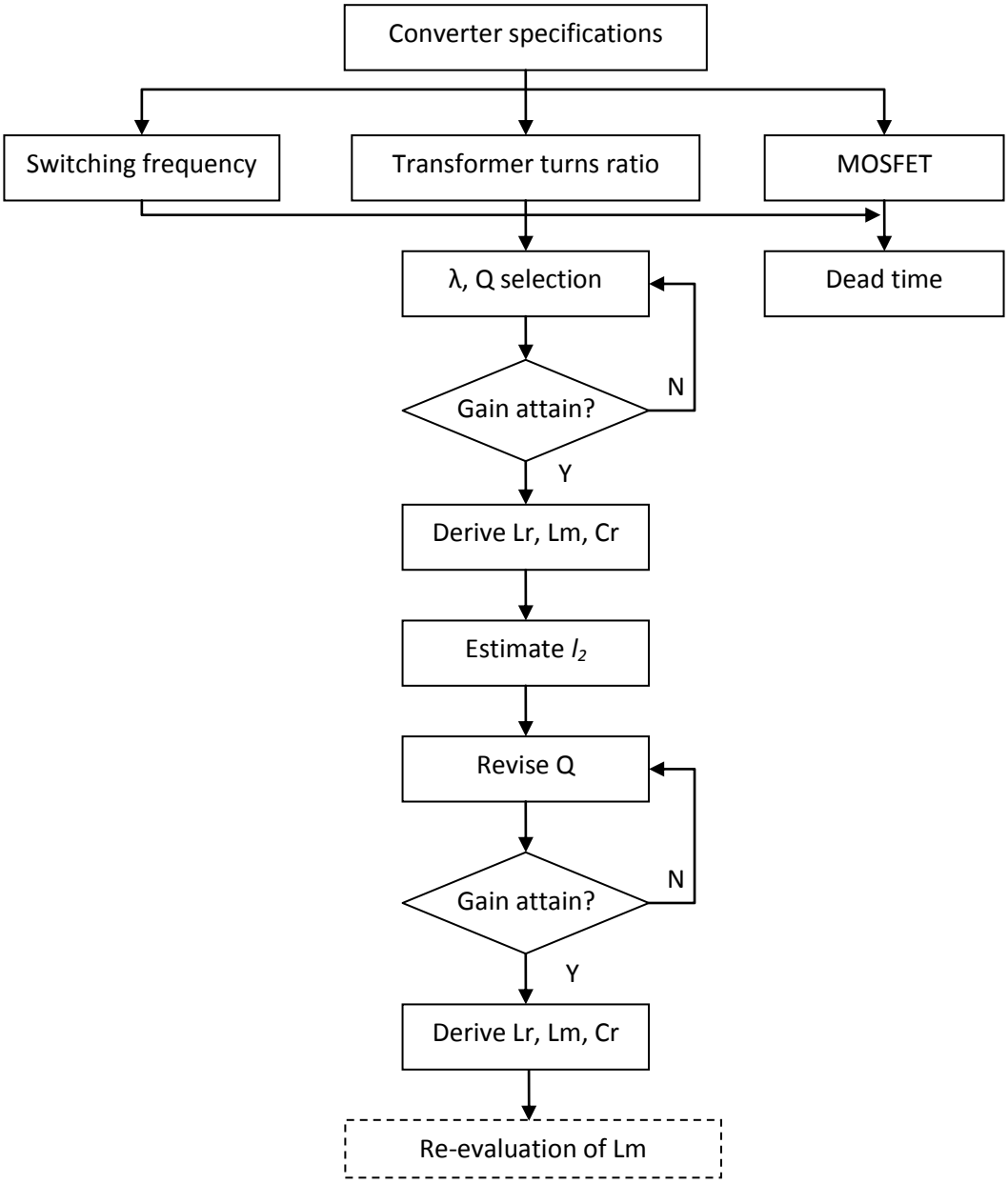


Figure 2-6. Proposed design procedures

Based on the converter specifications, it is possible to firstly fix the switching frequency range, the transformer turns ratio and select the adequate MOSFET. LLC's voltage conversion ratio analysis is established without considering the secondary parasite inductance, in order to get a design result for ideal resonant tanks. Based on the derived parameters, by considering the influence of secondary parasite inductance (l_2), the new voltage conversion ratio plot is built and the circuit quality factor value is revised to re-adapt the gain requirement. This design procedure considers fully the influence of secondary leakage

inductance and searches the optimal dimensioning results for improving the power factor and increasing power conversion efficiency.

The above procedures permits to get the optimized dimensioning results based on limited frequency to comply with large voltage range. The last step (necessary in several cases) is to adjust the Lm value based on the derived calculations to further improve its power factor. Increment of Lm improves the power factor, but reduces the input voltage variation range. Details of dimensioning the LLC cell will be presented and compared to search the optimum results at the following sections.

2.2.1 Equivalent circuit and frequency domain analysis

First harmonic analysis (FHA) method is a common method for establishing the equivalent electrical circuit of a LLC converter by approximating the voltage/current waveforms as first order sinusoidal wave, while neglecting the impacts of the other high order harmonics [2-15]. In order to get the equivalent model of the LLC resonant converter, several assumptions are adopted:

(1) The switching components, including the primary and secondary MOSFETs, are considered as ideal MOSFETs. The MOSFET's on resistance R_{dson}, parasitic capacitor C_{iss}, C_{rss} & C_{oss}, body diode's forward biased voltage are neglected.
(2) The magnetic components are considered as ideal components. Inductor's resistances, transformer's primary and secondary resistances are neglected. Transformer's leakage inductance is also neglected, except that the transformer's primary leakage inductance can be merged with the resonant inductance.
(3) The influence of the dead-time's length is neglected. In fact, its influence is rather limited when its length is far less than the switching period [2-16].

Referring to the Figure 1-13, the equivalent circuit of the LLC resonant converter can be presented in the Figure 2-7:

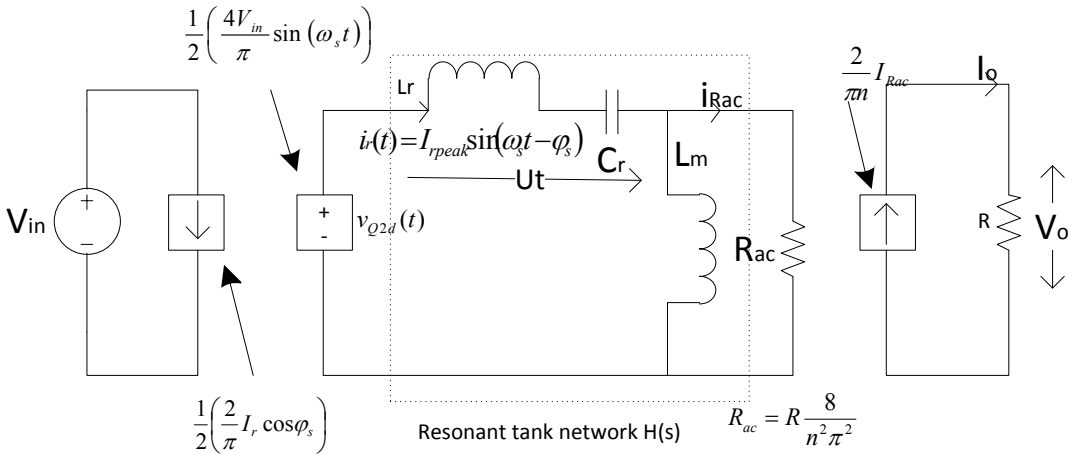


Figure 2-7. The equivalent circuit of the single cell LLC resonant converter

I_{rpeak} is the peak value of the resonant current in the resonant tank and $v_{QLds}(t)$ is the drain-source voltage of the MOSFET Q_L. φ_s is the phase shift between $i_r(t)$ and $v_{QLds}(t)$. $\frac{1}{\pi} I_r \cos\varphi_s$ signifies the average current debited from the DC source. R_{ac} signifies the equivalent resistance of the load resistance R transferred to the transformer's primary side, which can be obtained as follows:

$$R_{ac} = \frac{V_{Rac}}{I_{Rac}} = R\frac{8}{n^2\pi^2} \quad (2\text{-}1)$$

The amplitude of the fundamental series of the $v_{Rac}(t)$ can be expressed by equation (2-2).

$$\left|v_{Rac}(t)\right| = \frac{4V_o}{\pi n} \quad (2\text{-}2)$$

$\frac{2}{\pi n} I_{Rac}$ is the average rectified output current. Based on the above equations, the converter's global gain can be calculated as:

$$G_{global} = \frac{V_o}{V_{in}} = \frac{V_o}{I_o}\frac{I_o}{I_{Rac}}\frac{I_{Rac}}{V_{Rac}}\left(\frac{V_{Rac}}{V_{Q2d}}\right)\frac{V_{Q2d}}{V_{in}} = R\frac{2}{\pi n}\frac{\pi^2 n^2}{8R}\left\|H(s)\right\|_{s=j\omega s}\frac{4}{2\pi} = \frac{1}{2}n\left\|H(s)\right\|_{s=j\omega s} \quad (2\text{-}3)$$

Where the $\left\|H(s)\right\|_{s=j\omega_s}$ is the transfer function of the resonant tank, which can be presented by $G=||H(s)||$. The equation (2-3) signifies that the global gain of the resonant converter equals to the product between the DC gain of the resonant tanks H(s), the transfer ratio of the

transformer n and the gain of the half bridge converter 1/2, as shown in the following equation (2-4).

$$G_{global} = \frac{1}{2} n \left\| H(s) \right\|_{s=j\omega s} = \frac{1}{2} nG = \frac{V_o}{V_{in}} \quad (2\text{-}4)$$

The gain of the resonant tank at normalized frequency domain is represented in the equation (2-5):

$$G = \frac{1}{\left(1 + \lambda - \lambda \frac{1}{f_n^{\,2}}\right) + jQ\left(f_n - \frac{1}{f_n}\right)} \quad (2\text{-}5)$$

Where the $Q = \frac{\sqrt{L_r / C_r}}{R_{ac}}$, the quality factor of the resonant converter; $f_n = \frac{f_s}{f_r}$, the switching frequency after normalization; $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, the main resonant frequency; $f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}}$, second resonant frequency; $\lambda = \frac{L_r}{L_m}$, ratio between the leakage inductance and the magnetizing inductance.

The Figure 2-8 shows the DC gain characteristics of a LLC resonant converter under different Q values with λ=0.25.

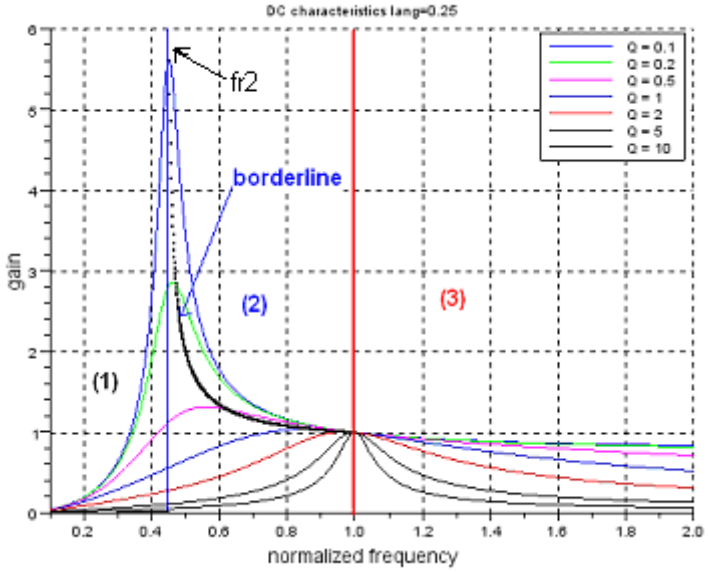
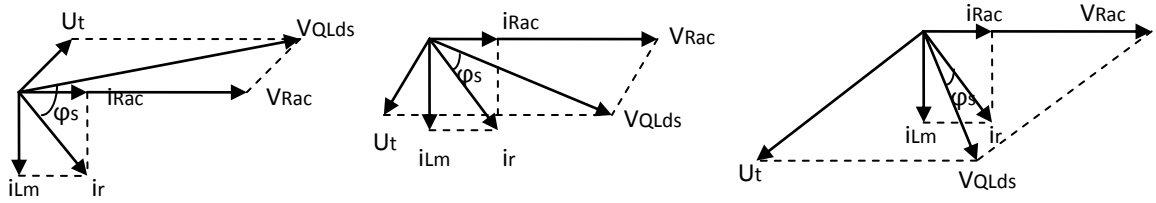


Figure 2-8. The DC gain characteristics of LLC resonant converter at λ=0.25

It is apparent that at f_n=1, the gain of different Q values are equal to 1, which is called the load independent point. The operation of LLC resonant converter can be divided to 3 different regions. In the region (1), the slope of the gain curve is positive and the resonant current leads the resonant voltage, thus the circuit is possible to operate in ZCS mode. Since the ZVS is highly preferred than ZCS for the switching of MOSFET, this operating region has to be avoided during all the operational frequencies. The region (2), which is separated from the region (1) by the plotted borderline and separated from the region (3) by the curve f_n=1, is the ZVS-BOOST region. The gain of the resonant tank at this region is higher than 1. In this mode, the transformer is not fully clamped by the load and the output current at the center-tapped secondary side is discontinuous. It has to be reminded that the region (2) only occurs for converters with a lower Q value. The region (3) is the ZVS-BUCK region. In this region, the transformer will be fully clamped by the load and the output current waveform is continuous.

To compare the different operational regions, the Figure 2-9 shows the vector diagram of the LLC circuit operating in ZVS-BUCK, ZVS-BOOST and ZCS region, respectively.



ZVS-BUCK (CCM) ZVS-BOOST (DCM) ZCS

Figure 2-9. The vector diagram of the LLC converter operating in different regions

v_{QLds} is a quasi-square wave produced by the half bridge inverter, with an amplitude $V_{in}/2$ and a first-order harmonic amplitude of $2V_{in}/\pi$. In ZVS-BUCK, as shown in Figure 2-9, while the operational frequency is above the resonant frequency, the resonant tank composed by L_r and C_r appears inductive and $\overrightarrow{u_t}$ leads $\overrightarrow{i_r}$ with $\pi/2$. The obtained $\overrightarrow{v_{QLds}}$ leads $\overrightarrow{i_r}$ with an important phase difference φ_s thus results in a low power factor. In ZVS-BOOST, as the operational frequency is below the resonant frequency, the resonant tank is capacitive and the tank voltage turns to the opposite direction. This results in a reduced phase difference φ_s and a higher power factor. As $P_{in} = v_{QLds} i_r \cos\varphi_s$, under a given input voltage and input power, a higher power factor is helpful to reduce the primary resonant current i_r thus reduce the power

loss at HV MOSFETs and transformer primary windings. This is one great advantage of operating LLC at ZVS-BOOST mode. Finally when the frequency continues to decrease, the resonant tank turns to be even more capacitive and finally the $\overrightarrow{v_{QLds}}$ lags $\vec{\imath_r}$, which enters to ZCS mode. In all, operating in the ZVS-BOOST region is possible to limit the converter's switching frequency between two resonant frequencies f_r and f_{r2}, and can also improve the converter's quality factor, which is highly preferred in attaining the requirement of designing HV/LV DCDC converters in electric automobile industries: limited operational frequency range, large input voltage variation. Thus the ZVS-BOOST region is selected in designing this prototype.

As depicted in the Figure 2-8, the selection of Q value greatly influences the voltage gain at the ZVS DCM region. The voltage gain attained by the LLC resonant converter increases with Q decreases. Besides, the lower the Q value, the nearer that the maximum gain will approach the second resonant frequency. For its value selection, Q should be selected sufficiently low to satisfy the enough gain requirement at minimum operational frequency, but it should not be selected too small. A smaller Q will result in a lower impedance characteristic of the resonant tank and a poorer power factor. Thus the Q parameter should be properly selected to attain the gain requirement, while keeping a high quality factor.

The *G-f* characteristics of the LLC converter at different λ values are represented in the following figures.

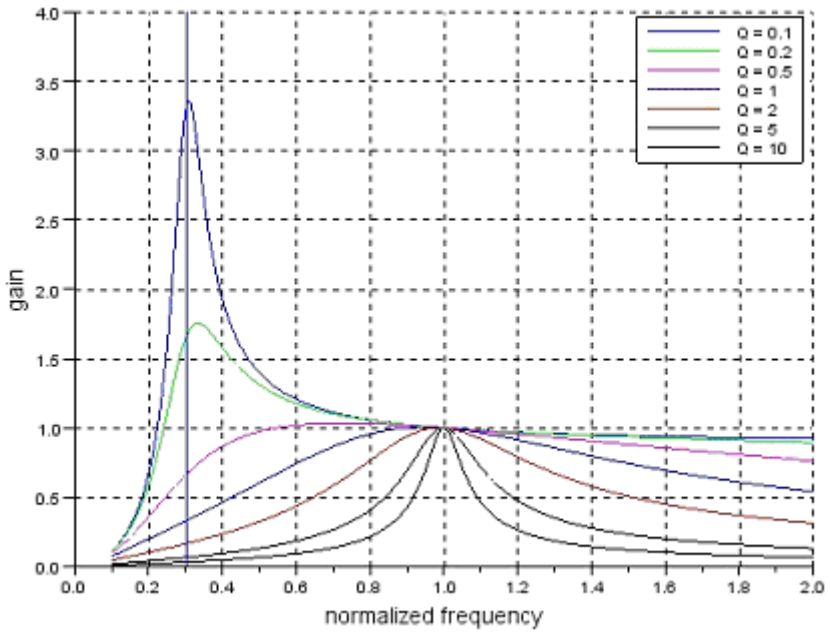


Figure 2-10. The DC gain characteristics of LLC resonant converter at λ=0.1

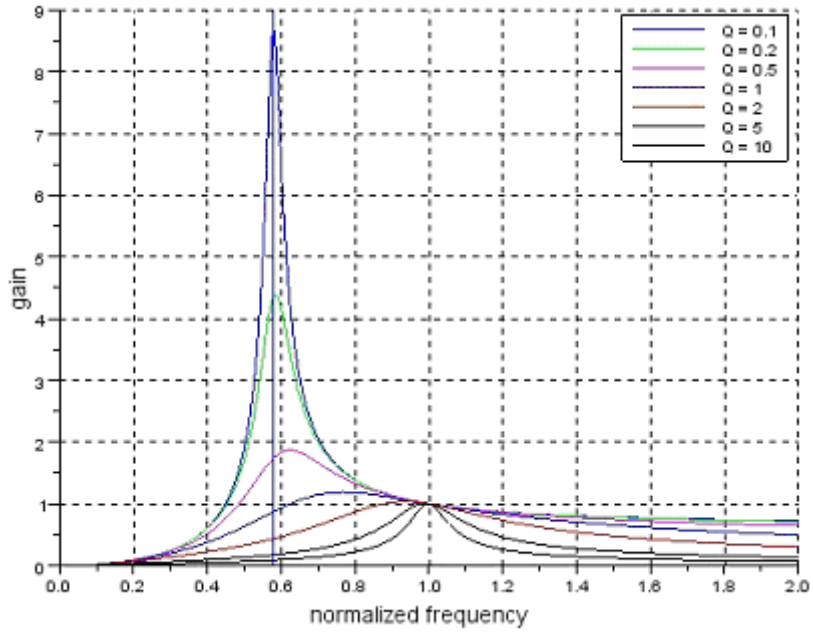


Figure 2-11. The DC gain characteristics of LLC resonant converter at λ=0.5

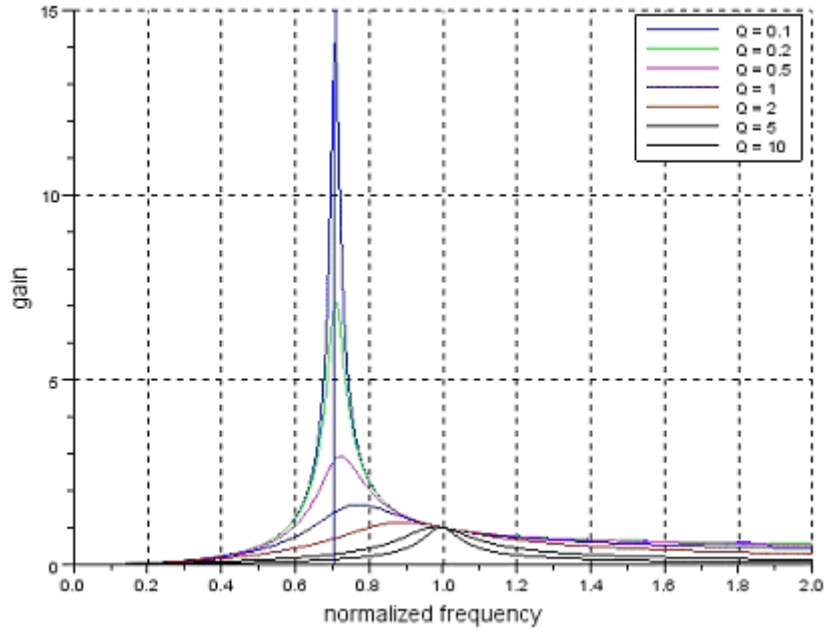


Figure 2-12. The DC gain characteristics of LLC resonant converter at λ=1

As shown in the above figures, a lower λ value results in a left-shift of the second resonant frequency and an expansion of the ZVS-BOOST operation range. It seems that a lower value is preferable to obtain a large ZVS-BOOST zone; however, if the λ value is selected too small, the converter's minimum operational frequency should drop to a low value to exhibit

high voltage transfer ratio with low Q, the benefit of LLC resonant converter working at high frequency cannot be maintained. Furthermore, low λ value also causes more discontinuous current at the secondary windings thus more conduction loss. In conclusion, the λ value is ideally to be selected to assure the second resonant frequency a little lower than the converter's minimum switching frequency.

From the above analysis, it is clear that the λ value decides the operational frequency range and the Q value decides the maximum gain that can be achieved at the minimum operational frequency. Thus, in order to keep a large voltage regulation capability at a specified operational frequency range, it is better to select firstly the λ value according to the frequency range definition and then find an adequate Q value to attain the maximum gain requirement at minimum operational frequency.

2.2.2 Circuit design

As described in the above section, ZVS-BOOST region is selected for this LLC converter designing. The aim of this circuit design is to find the optimal electrical parameters to better fit the requirement of large input variation range, limited operational frequency and high quality factor. In LLC resonant converter, the two operational frequency ranges of ZVS-BUCK and ZVS-BOOST are separated by the resonant frequency. To ensure the operation of ZVS-BOOST among all the operational frequency ranges, the maximum switching frequency should not be set to a frequency higher than the resonant frequency f_r. In fact, it is optimal to set the resonant frequency to the same as the maximum switching frequency (265kHz) which will greatly simplify the design procedures so that the voltage conversion ratio at this frequency depends only on the transformer ratio. Thus,

$$f_r = f_{s\max} \quad (2\text{-}6)$$

The load independent point is set to get the minimum output voltage at maximum input voltage, the transformer's transfer ratio can then be selected as follows:

$$n = \left(\frac{N_2}{N_1}\right) \approx \frac{V_{o\min}}{V_{in\max}/2} \quad (2\text{-}7)$$

½ represents the gain of the half bridge and N_2, N_1 should be integer values. The obtained n value is 1/16, with N_2=1, N_1=16.

As discussed in the above section, the selection of the ratio between resonant inductor and magnetizing inductor greatly influences the ZVS-BOOST region's width. To keep the circuit's operation at ZVS-BOOST mode, the second resonant frequency f_{r2} should be inferior to the minimum switching frequency 150kHz.

$$\frac{f_{r2}}{f_r} < \frac{f_{s\min}}{f_{s\max}} \Rightarrow \lambda < \frac{f^2{}_{s\min}}{f^2{}_{s\max} - f^2{}_{s\min}} \quad (2\text{-}8)$$

As discussed in the above section, the λ should be chosen to a value slightly less than the above calculated result. In this design, λ = 0.33.

Set the load independent point to ensure the sufficient output voltage at the maximum input voltage (V_{inmax}, V_{omin}) and the point at f_{smin} should be set as (V_{inmin}, V_{omax}). Thus a sufficient gain of

$$g = \frac{V_{o\max} \cdot V_{in\max}}{V_{in\min} \cdot V_{o\min}} \quad (2\text{-}9)$$

should be attained at f_{smin} to get an enough voltage gain. By referring to the *G-f* plot, a *Q* value can be found to meet the desired gain requirement, illustrated in the Figure 2-13. It has to pay attention that under a same λ value, a higher *Q* helps to improve the power factor thus the *Q* value should be selected as high as possible. *Q*=0.25 is adopted in this project. With the obtained parameters for λ and *Q* values, the resonant cell's voltage conversion ratio characteristics and operational regions can be plotted in the following figure.

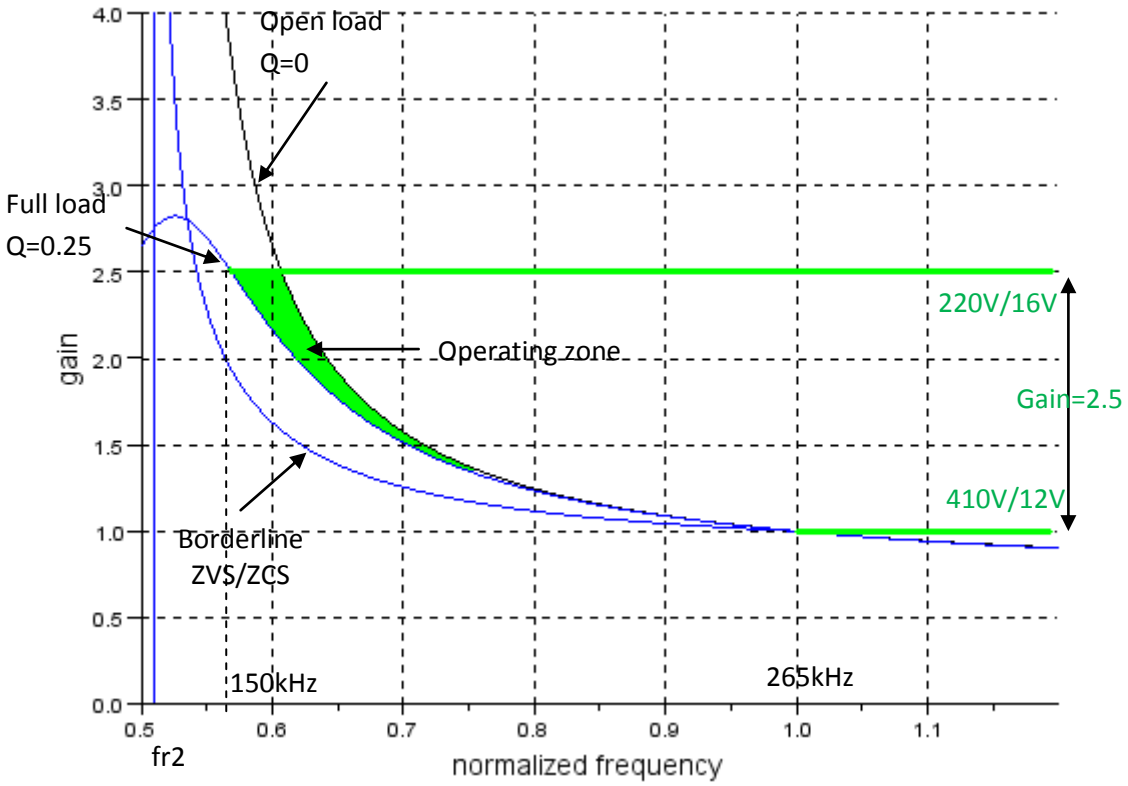


Figure 2-13. The operating zone of the designed LLC resonant power cell

The nominal output current and the nominal load can be derived from the following equations:

$$I_o = \frac{P}{V_o} \quad (2\text{-}10)$$

$$R_{out} = \frac{V_o}{I_o} \quad (2\text{-}11)$$

Based on the definition of the quality factor and resonant frequency of a resonant circuit, the parameters for resonant inductor and resonant capacitor can be developed as:

$$\begin{cases} Q = \dfrac{\sqrt{L_r / C_r}}{R_{ac}} \\ \omega_r = \dfrac{1}{\sqrt{L_r C_r}} \end{cases} \Rightarrow \begin{cases} L_r = R_{ac} \dfrac{Q}{\omega_r} \\ C_r = \dfrac{1}{\omega_r^{\,2} L_r} \end{cases} \quad (2\text{-}12)$$

Once the resonant inductance is obtained, the transformer's magnetizing inductance can be calculated by the following equation:

$$L_m = \frac{L_r}{\lambda} \quad (2\text{-}13)$$

The derived circuit parameters are: Lr=5μH, Lm=15μH, Cr=80nF.

2.2.3 Influence of secondary leakage inductance

The primary leakage inductance of a transformer can be integrated with the series resonant inductor; however, the influence of the secondary leakage inductance can neither be integrated nor neglected. Secondary leakage inductance exists in all transformers, whose value depends on the coupling factor of primary and secondary windings and its external wire length. In this project, an additional wire length of 16cm is needed at the transformer's secondary side to connect the LV MOSFET module and the output PCB filter card, while the leakage inductance is measured to be l_2=123nH. In case of high frequency, high power applications, the impedance of this secondary leakage inductance is increasing (116mΩ at 150kHz, 193mΩ at 250kHz) and even rise up to be the same order as the nominal load R=160mΩ. Its effect should thus be considered in the design and dimensioning of power cell parameters. Figure 2-14 shows the AC equivalent circuits of an ideal LLC resonant cell and a LLC cell including secondary leakage inductance.

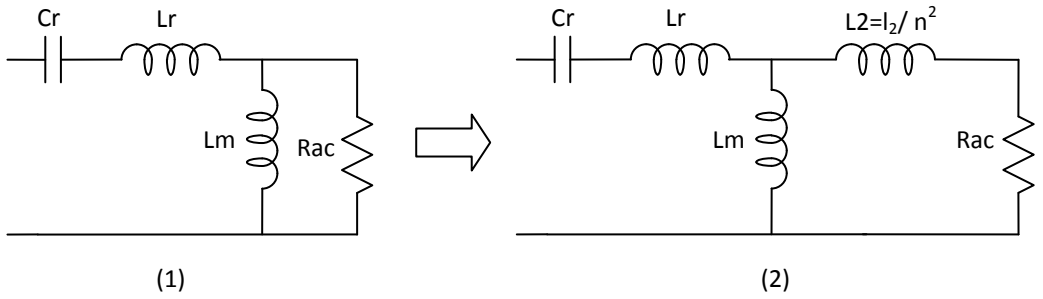


Figure 2-14. Equivalent circuit of the LLC resonant converter cell without (1) or with (2) secondary leakage inductance

The voltage conversion ratio of LLC converter including the leakage inductance can be written as:

$$G = \frac{Rac}{Rac\left(1-\frac{\omega_m^{\,2}}{\omega^2}\left(1-\frac{\omega^2}{\omega_r^{\,2}}\right)\right)+j\omega\left(n^2 l_2\left(1-\frac{\omega_m^{\,2}}{\omega^2}\left(1-\frac{\omega^2}{\omega_r^{\,2}}\right)\right)-L_m\frac{\omega_m^{\,2}}{\omega^2}\left(1-\frac{\omega^2}{\omega_r^{\,2}}\right)\right)} \quad (2\text{-}14)$$

Where $\omega_r = \frac{1}{\sqrt{L_r C_r}}$; $\omega_m = \frac{1}{\sqrt{L_m C_r}}$; L_2 is the secondary leakage inductance transferred to the primary side, $L_2 = \frac{l_2}{n^2}$. The equation (2-14) is firstly proposed in [2-18]; however, the author neither continues to fully explore the characteristics of LLC converter including its secondary leakage inductance, nor proposed how does this leakage inductance affects converter's parameter dimensioning in obtaining an optimal designing result. In the following part, the influence of this secondary leakage inductance will be fully analyzed, particularly in case of L_2 close to Lm, which always happens under high power and large input voltage variation range conditions. In order to study the influence of secondary leakage inductance analytically; it is better to normalize the above equation (2-14) and to represent it in the following format:

$$G = \frac{1}{\left(1+\lambda-\lambda\frac{1}{f_n^{\,2}}\right)+jQ\left(\left(\frac{L_2}{L_m}\left(1+\frac{1}{\lambda}\right)+1\right)f_n-\left(\frac{L_2}{L_m}+1\right)\frac{1}{f_n}\right)} \quad (2\text{-}15)$$

The graph of DC gain characteristics is plotted in Figure 2-15.

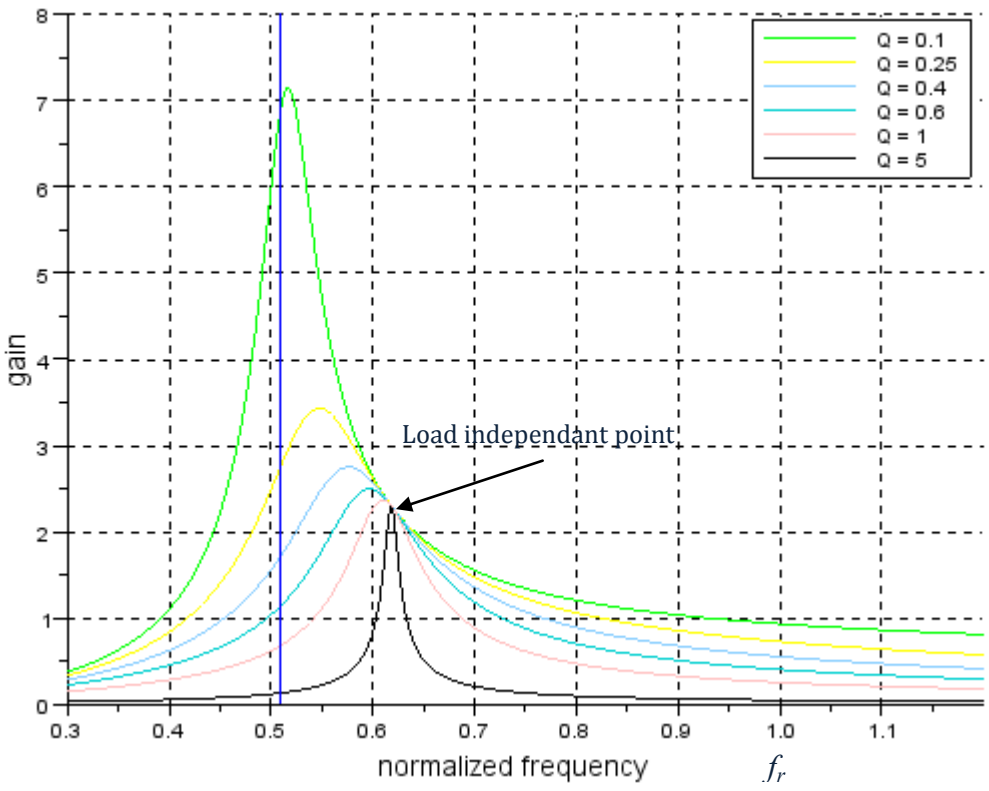


Figure 2-15. DC gain characteristics of LLC resonant converter with l_2=120nH

Several conclusions can be drawn based on the developed equation:

(1) At no load, Q=0, the voltage gain remains the same as in ideal LLC resonant converters. This is easy to understand since there is no current in the secondary leakage inductance.

(2) At the normalized frequency f_n=1, the gain expression can be written as:

$$G = \frac{1}{1 + jQ\left(\frac{L_2}{L_r} + 1\right)} \quad (2\text{-}16)$$

Due to the imaginary part in the above equation, the gain at f_n=1 is less than 1, except for open circuit. This means that the main resonant frequency is no longer a load independent point. At a heavier load (low *R*ac, high *Q*), the gain is lower. This is due to the fact that at lower *R*ac, the leakage inductance's impedance is closer to the load resistance and it plays a role of voltage divider.

(3) By imposing the imaginary part of equation (2-15) equal to 0, it is possible to derive the new load independent point as follows:

$$f_{ind} = \sqrt{\frac{\frac{L_2}{L_m} + 1}{\frac{L_2}{L_m}\left(1 + \frac{1}{\lambda}\right) + 1}} \quad (2\text{-}17)$$

From equation (2-17), if $L_2 << L_m$, the f_{ind} remains close to 1 and the converter's load independent point is not greatly influenced by this leakage inductance. In this case, the secondary leakage inductance has very limited influence to the characteristics of LLC power cell. But in this converter design, L_2=30µH, which is even higher than the pre-designed Lm value Lm=15µH. As a result, the DC gain characteristics of this resonant cell are greatly influenced. The gain at the new load independent point can be obtained as:

$$G_{f=find} = \frac{L_m + L_2}{L_m} \quad (2\text{-}18)$$

Equation (2-18) shows that the voltage conversion gain at load independent point including secondary leakage inductance is higher than 1, moreover, it increases with the increase of L_2. By developing the equation (2-17), the frequency at the independent point can be derived as:

$$f_{ind} = \frac{1}{2\pi\sqrt{C_r(L_r + L_m // L_2)}} \quad (2\text{-}19)$$

From equation (2-19), it is obvious that the new load independent point appears at a frequency where Cr is in resonant with all the three inductors. The new independent frequency locates between the first resonant frequency and second resonant frequency: $f_r > f_{ind} > f_{r2}$. In conclusion, the leakage inductance moves the load independent point to left with a gain higher than one.

(4) As to a same *Q* value, the maximum voltage conversion ratio is increased by including secondary leakage inductance compared with ideal LLC. As studied in the above section, the maximum gain obtained in ideal LLC resonant cell with *Q*=0.25 is G=2.8 at f_n=0.55 (referring to Figure 2-13). In comparison, this G is raised up to 3.4 under the same Q value (referring to Figure 2-15). The added leakage inductance increases the maximum gain, but decreases the power factor according to discussions at the part 2.2.1. Gain=3.4 is far higher than required voltage conversion ratio of 2.5. It is possible to continue with the actual *Q* value, but the converter will encounter serious power factor problems and thus a worse power efficiency. Increasing the *Q* value from 0.25 to 0.4 is a good solution to reduce the gain and improve the power factor.

The phase difference between the half bridge middle point voltage V_{QLds} and resonant current waveform *ir* can be analysed by evaluating the input impedance of resonant power cell with $\varphi = angle(Z_{in})$, of which the results are shown in the following figure.

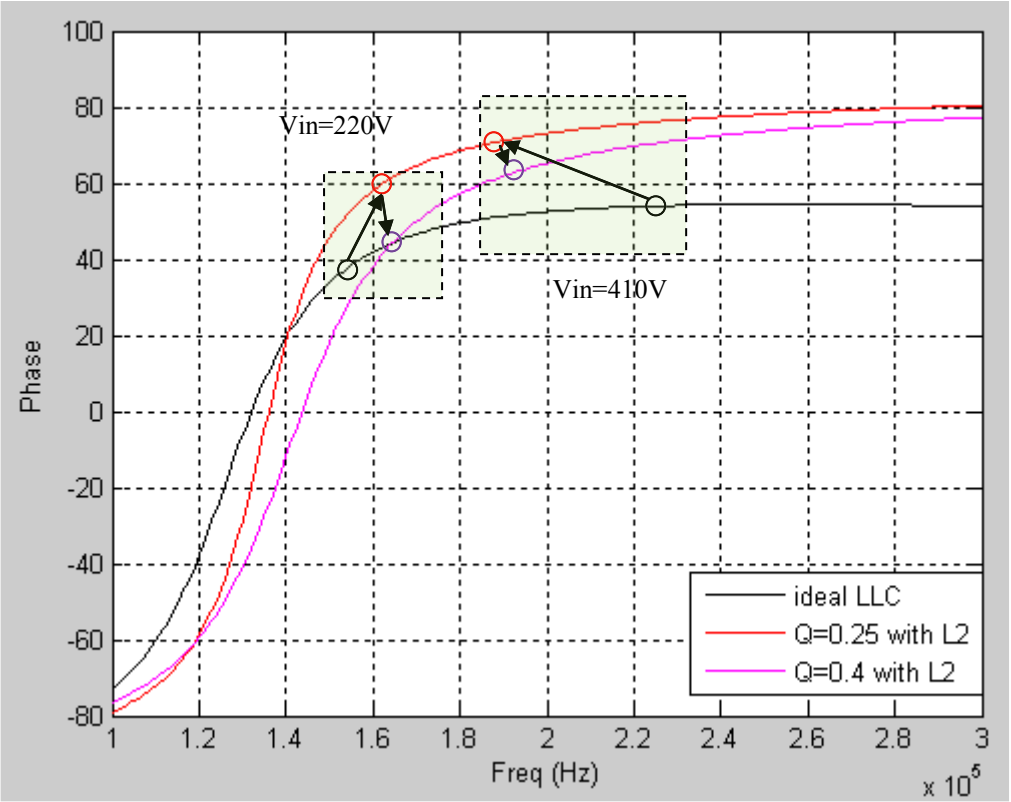


Figure 2-16. Operating points transition at nominal power under two different input voltages (Vin=220V, Vin=410V, separately)

In Figure 2-16, a positive phase difference means the resonant current lags the half bridge voltage, vice versa. For an ideal LLC operating at Vin=220V with nominal power, a phase difference of 38º is observed (cosφ=0.79). After including the secondary leakage inductance, the operating point is shifted to the red point where Δφ=60º, which greatly deteriorates its power factor (cosφ=0.5). Adopting a higher Q=0.4 helps to move the operating point to a reduced phase difference Δφ=45º (purple point, cosφ=0.71). At Vin=410V, an ideal LLC converter operates at 223kHz with a Δφ=54º (cosφ=0.59). By including the secondary leakage inductance, a higher gain needs to be developed thus the operating point shifts to 187kHz with Δφ=71º (cosφ=0.33). Increasing the quality factor from 0.25 to 0.4 makes the operating point shift to 192kHz where Δφ=62º (purple point, cosφ=0.47).

With the revised *Q* value, it is possible to recalculate the power cell's parameters. Finally the obtained power cell parameters are: Lr= 7.5uH, Lm=24uH, Cr=50nF. The voltage conversion ratios with the revised resonant tank circuit parameters under different load conditions are plotted in the following figure.

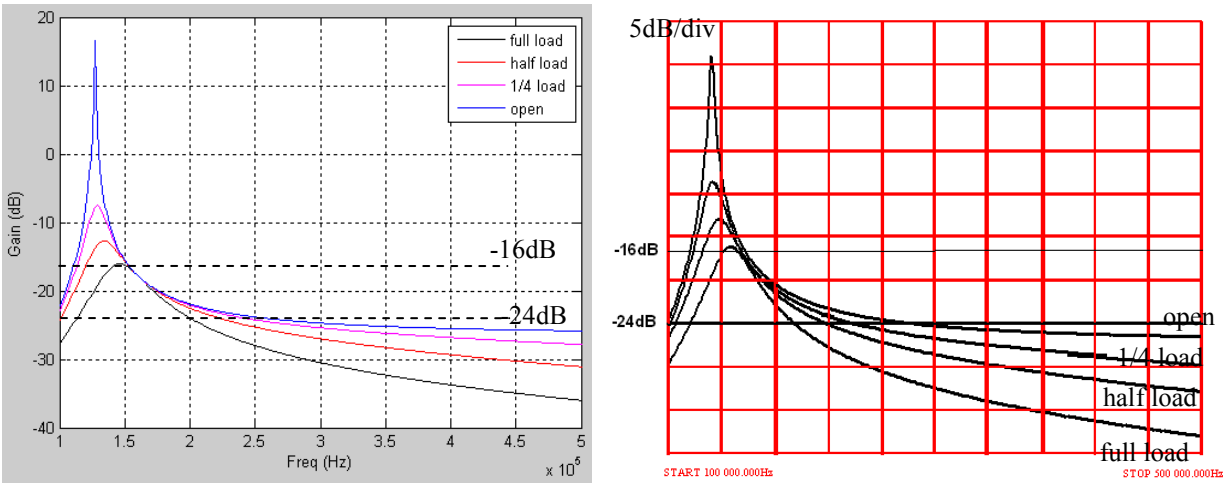


Figure 2-17. Theoretical and experimental voltage conversion ratio under different loading conditions, including transformer's secondary leakage inductance

In the above calculation and measurement, the transformer's conversion ratio is included. -24dB=20log(1/16) signifies the unit voltage gain, -16dB=20log (2.5/16) signifies the targeted gain of 2.5, with n=1/16. As plotted, the resonant tank operates between 150kHz and 265kHz, and is capable of attaining a sufficient gain=2.5 at 150kHz. Experiments are launched to verify the voltage conversion ratio characteristics with the real transformer and inductor under different load conditions, of which the results are in good accordance with the theoretical results, which verifies the established resonant cell model. It is also apparent that the secondary leakage inductance makes the operation region of LLC narrower.

The above part shows the influence of secondary leakage inductance to the parameter dimensioning of resonant power cells, it is also interesting to study the consequences of leakage inductance on circuit operation and dimensioning of power components.

(1) By including the secondary leakage inductance into consideration, the converter operates also in ZVS-BOOST mode, but not fully DCM. At low load, the leakage inductance has limited influence to the circuit operation and the circuit operates still in DCM. With the increase of power load and decrease of load resistance, the output current increases and leakage inductance slows down the secondary current waves then the circuit operates in CCM. Working in CCM reduces the RMS value of secondary current thus reduces the conduction power loss at LV MOSFETs.

(2) Secondary leakage inductance increases the AC voltage amplitude at the transformer secondary side and thus increases the transformer's core loss. Due to a half sinus current

across the leakage inductor, a sinus voltage u_{l2} is developed. The transformer's secondary voltage u_{T2} thus sees a combination of the voltage u_{l2} and u_o, as shown in Figure 2-18. Besides, due to a CCM operation, the magnetizing or demagnetizing time duration is longer than DCM. The Bpk is then increased from 100mT to 150mT (simulated with E42/21/15, Se=178mm^2).

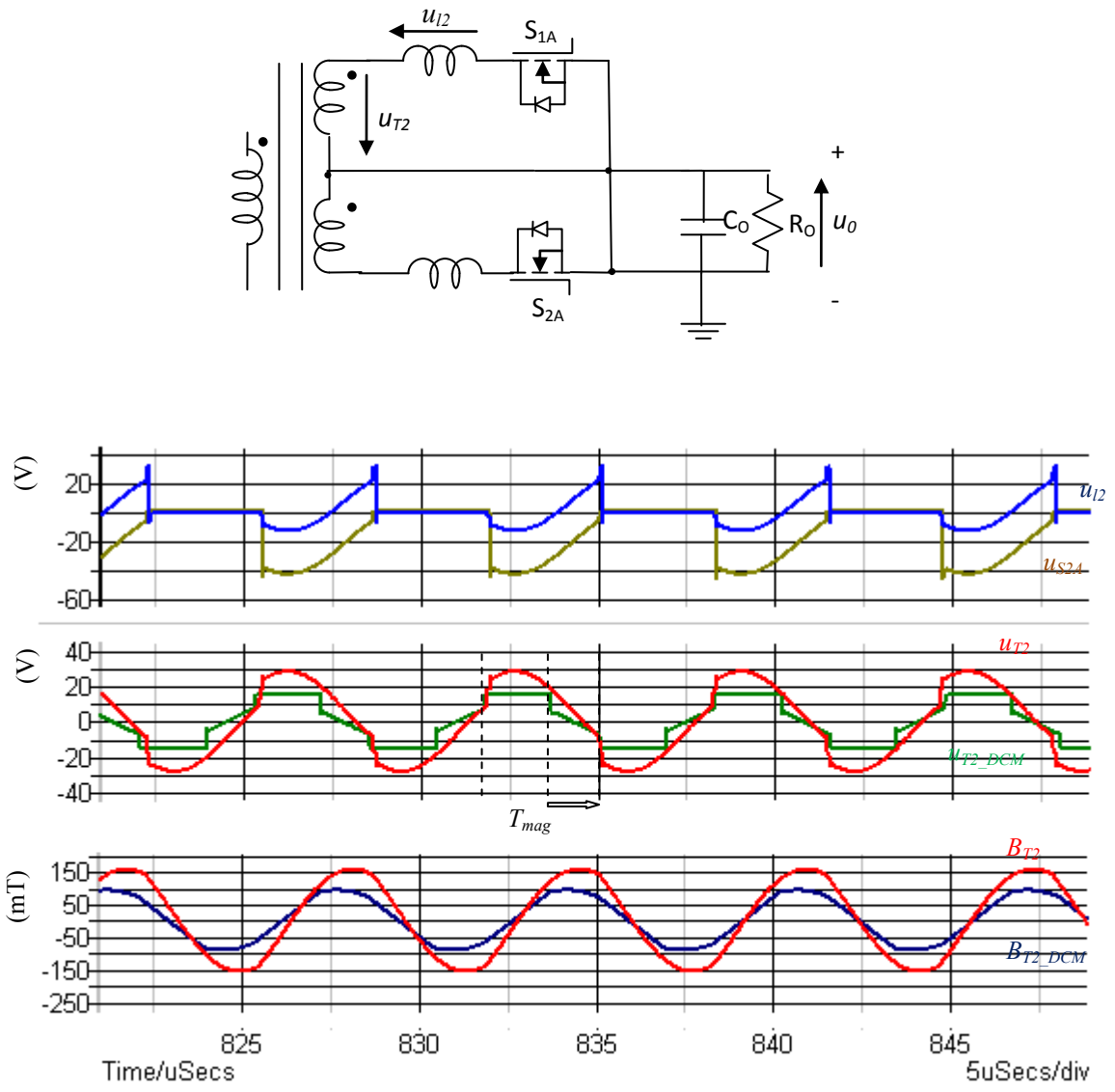


Figure 2-18. Waveforms of circuit operation considering the secondary leakage inductance

(3) Secondary leakage inductance develops a sinus voltage and this voltage is reflected to another SR MOSFET. For example, when S_{1A} is switched on, S_{1A} suffers a voltage combination of u_{T2}+u_o. Since u_{T2} is deformed by the secondary leakage inductance, SR MOSFET may need to support more withstand voltage. In this project, the withdrawn voltage

is increased from 30V to 40V. LV MOSFET with withstand voltage of at least 60V should be selected rather than 40V considering a design margin.

2.2.4 Re-evaluation of Magnetizing Inductance vs. input voltage regulation capability

Following the above calculations, one can derive ameliorated circuit parameters of resonant tanks to comply with large input voltage variation at limited frequency range. Although that the power factor has been ameliorated by increasing *Q* value following the above process, the obtained result still drops into a low Lm value, Lm=24μH. Simulation shows that the rms resonant current at Vin=330V is 17A and the rms magnetizing current is 11.9A. The magnetizing current occupies a large fraction of resonant current and the overall performance is far from being ameliorated.

The most efficient way of improving the power factor is to increase the magnetizing inductance Lm to reduce the reactive power, but the input variation range will also be reduced. Large Lm makes the converter has insufficient gain to be able to operate at Vinmin. As a result, a BOOST PFC converter should be connected at the input of LLC, shown as follows:

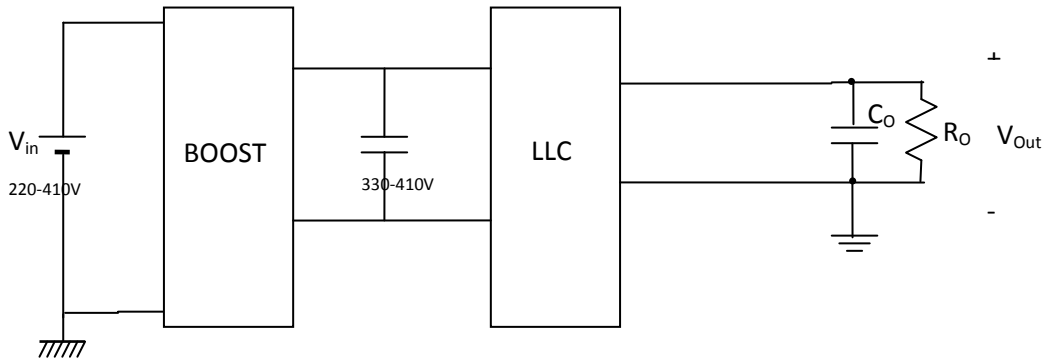


Figure 2-19. Proposal of BOOST+LLC to improve the power factor

As shown in the above figure, the input voltage variation range is reduced to 330-410V. For input voltage Vin less than 330V, the BOOST converter operates to increase the voltage to 330V; for Vin higher than 330V, the BOOST converter is inactive and the input voltage is added directly to LLC (with a diode voltage drop). The breakpoint of 330V is selected according to the charging characteristics of battery in electric vehicles.

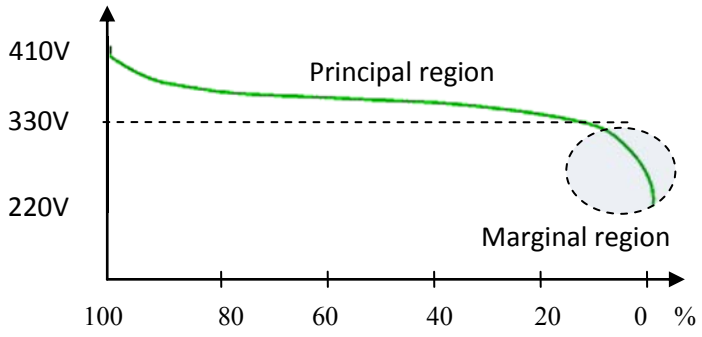


Figure 2-20. Typical state-of-charge (SOC) of a lithium ion battery in electric vehicles

For Lithium ion battery, principally, the battery works with a voltage higher than 330V. When the battery is discharged to less than 10%, its voltage falls from 330V to 220V rapidly. The operation range of [220V 330V] is in fact a marginal operation region of the proposed converter. For most of the time, the BOOST converter is not activated. A comparison of selecting different Lm values is shown at the following table.

Table 2-2. Comparison of different selections of Lm with loss predicted for Vin=220V, one cell

Lm selection	1. Lm=24μH	2. Lm=42μH	3. Lm=75μH
λ value	λ=0.31	λ=0.18	λ=0.1
Air-gap length	3.96mm	1.98mm	0.90mm
Vin reg. capability	[220V 410V]	[330V 410V]	[380V 410V]
Boost needed	No	Yes	Yes
BOOST start at	Never	SOC< 10% BOOST seldom on	SOC<90% BOOST always on
BOOST loss	0	15W	15W
Trf pri. Conduction loss	10.5W	3.9W	3.0W
MOSFET loss x2	18.5W	6.86W	5.14W
Eddy current loss	5.8W	1.5W	0.8W
Inductor loss	9.50W	3.81W	2.43W
ZVS HV MOSFET	Yes	Yes	Lost at low load
Total loss balance	0W	-13.23W	-17.93W

With Lm=42µH, the rms resonant current is reduced to 12A with 6A as rms magnetizing current. A reduction of resonant current decreases the conduction loss of HV MOSFETs, transformers and inductors. Furthermore, the air-gap length can be reduced to a half, which reduces greatly the winding's eddy-current loss (referring to chapter 4). Considering the overall loss, although the BOOST converter introduces an extra 15W loss, the whole system still gains more loss reduction of 13.23W (~1%) from the other components. For input voltage higher than 330V, the BOOST converter is off, the converter benefits even more efficiency improvement (>2%) in this case.

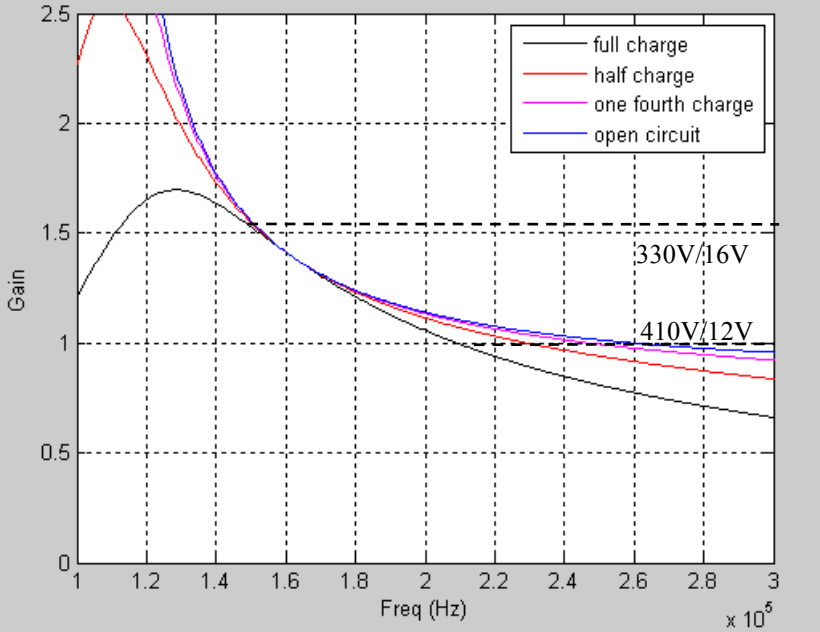


Figure 2-21. Voltage conversion ratio of modified LLC resonant cell with Lm=42µH

If the Lm is further raised to 75µH, the reactive current can again be reduced. However, too low reactive current makes it difficult to exhibit ZVS at full operation range. The dead-time should be increased, if not, the ZVS at light load maybe lost. Another disadvantage is that with Lm=75µH, the BOOST shall operate when SOC<90%, which means the BOOST should always be activated and this sacrifice the overall efficiency at HV battery's principal operational region.

In this dissertation, transformers with Lm=42µH and Lm=24µH are both built to verify the efficiency prediction of the LLC. Only the LLC conversion part is designed and built as prototype, the BOOST PFC is for fictive analysis and will not be built.

Following the above analysis, it is not a sensible idea to integrate all the functions of a DCDC into the LLC converter, but design the LLC converter to target a high efficiency at a reduced input voltage range with a BOOST PFC to broaden the input voltage regulation capability. This structure also brings us the design flexibility: if another car fabricant specifies an input voltage different from the prototype, we can re-design the BOOST PFC part only, without changing too much the design of the LLC.

2.2.5 ZVS condition fulfilment

To keep the correct ZVS during all ranges of input voltages and output powers, it is necessary to ensure that the ZVS equivalent capacitor across switching MOSFETs can be fully charged or discharged during the dead time. The lowest ZVS current happens at the maximum operational frequency and zero load condition. At no load, there is no current transferred to the secondary side and the current in the tank is just the magnetizing current of transformer. In each half-cycle, the resonant current is a linear straight line as the clamped voltage charged the magnetizing and resonant inductance, the minimum instant resonant current value at dead time for ZVS (I_{ZVS}) can be calculated as follows:

$$\left(L_m + L_r\right) \cdot \frac{I_{ZVS} - (-I_{ZVS})}{T/2} = V_{in\min} \Rightarrow I_{ZVS} = \frac{V_{in\min}}{4 f_{\max}\left(L_r + L_m\right)} \quad (2\text{-}20)$$

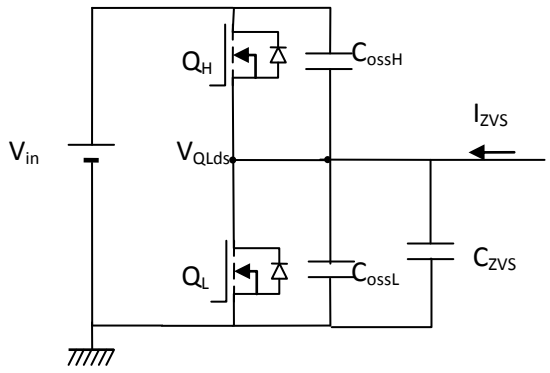


Figure 2-22. ZVS operation at the half bridge middle point

The obtained ZVS current is I_{ZVS}=6.6A. At the dead time, ZVS current charges one MOSFET's output capacitor and discharge the other. An additional ZVS capacitance is always added in order to limit the maximum dv/dt. This ZVS capacitor can either be directly paralleled with Q_{LA} or be divided into two capacitors and paralleled with both Q_{HA} and Q_{LA}. The total capacitance can be obtained as:

$$C = C_{ZVS} + Coss_L + Coss_H \quad (2\text{-}21)$$

Unlike linear capacitors whose capacitance is independent of the applied voltage, the Coss of MOSFET is a nonlinear capacitance, with its value as a function of V_{DS}. In this project, Super-junction MOSFET STW88N65M5 (650V, 24mΩ, TO247) is selected due to its low Rdson value and high dv/dt capability, of which the Coss vs. Vds relationship is shown as follows:

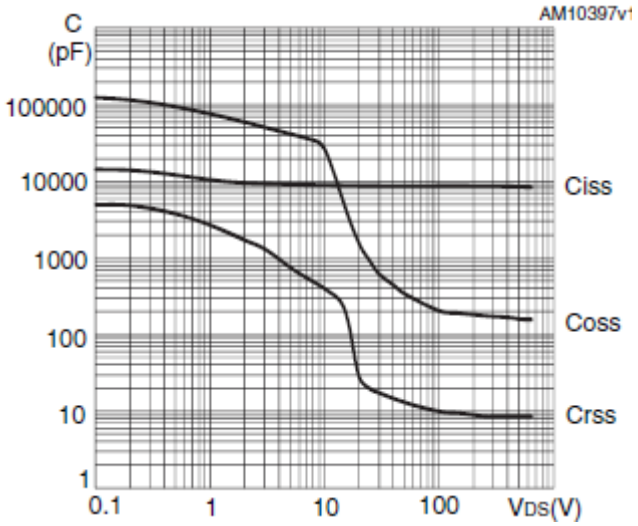


Figure 2-23. Capacitance variations of MOSFET STW88N65M5 vs. Vds

As reported in Figure 2-23, super-junction MOSFET STW88N65M5 performs high nonlinear capacitance property and it is hard to specify the Coss of super-junction MOSFET by a constant value. The Coss at low Vds is close to 120nF while at high Vds is close to 0.2nF. When one MOSFET is charging from 0V, another MOSFET is discharging from Vin and Coss of the latter can be neglected. Thus only one MOSFET's Coss need to be considered at the start of charging. In order to study its characteristics, it is possible to divide the charging into several periods that each period can be considered with linear capacitance properties, shown as in the following figure.

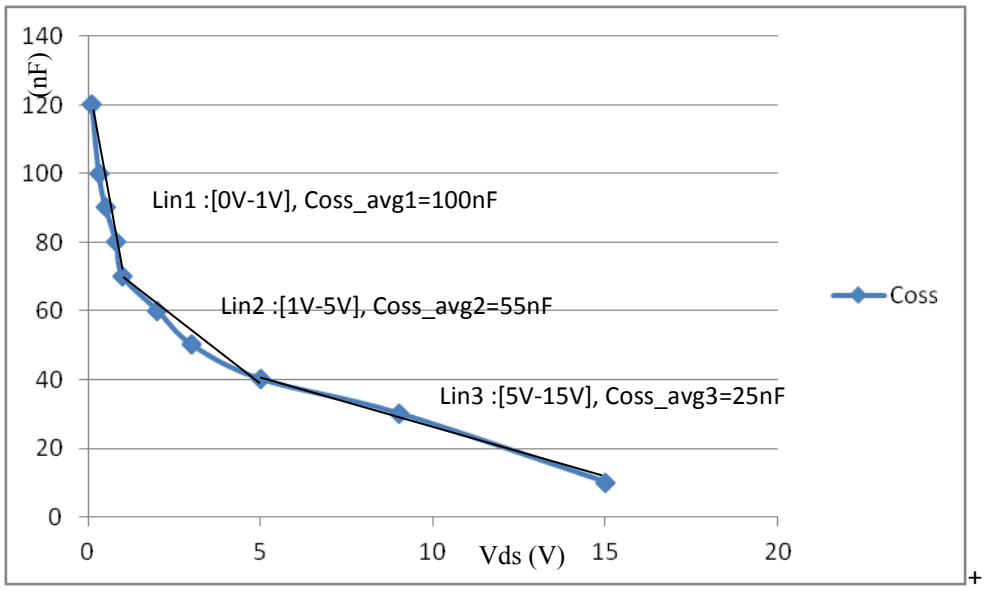
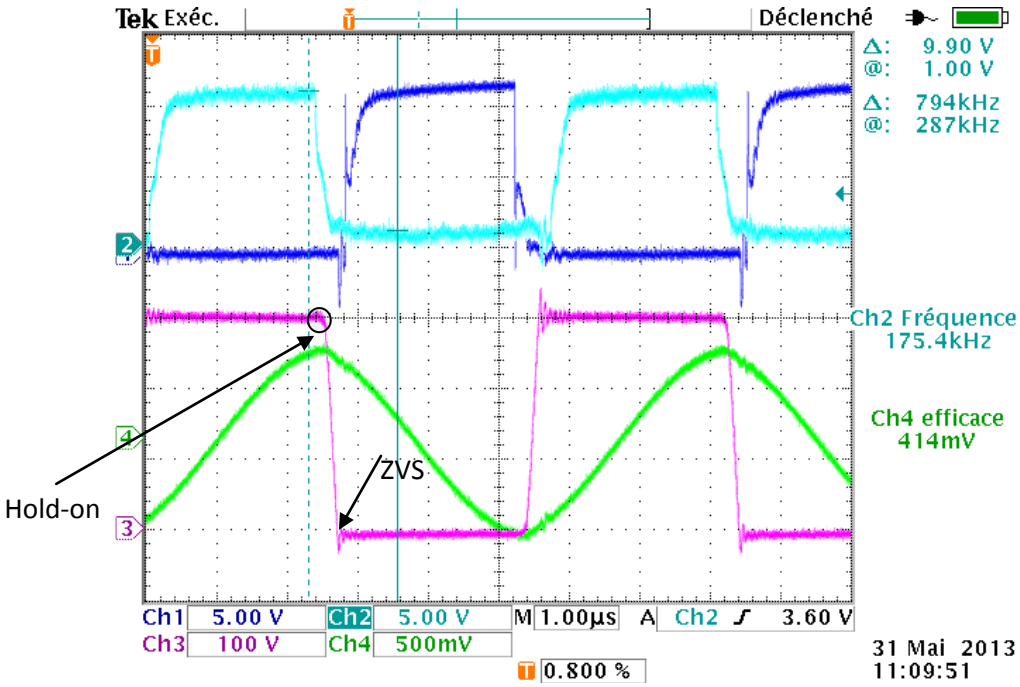


Figure 2-24. Capacitance variations of MOSFET STW88N65M5 vs. Vds

The beginning of the capacitor charging can be approximated into three periods with linear capacitances. The time for v_{QLds} rise from 0V to 15Vcan be calculated as the sum of the time for capacitor charging from ΔV_1: [0 1V], ΔV_2: [1V, 5V] and ΔV_3: [5V 15V], respectively.

$$t_{ch} = t_1 + t_2 + t_3 = C_{oss\_avg1}\frac{\Delta V_1}{I_{ZVS}} + C_{oss\_avg2}\frac{\Delta V_2}{I_{ZVS}} + C_{oss\_avg3}\frac{\Delta V_3}{I_{ZVS}} \quad (2\text{-}22)$$

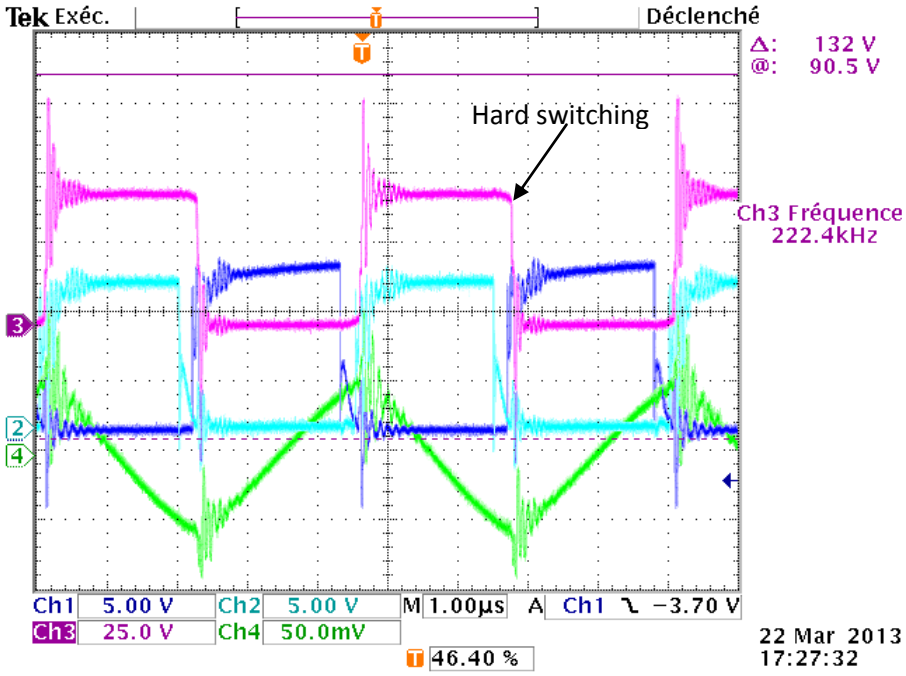
The derived charging time tch=85ns. During this time period, the MOSFET drain-source current remain slightly changed.From V_{QLds}= 15V, the total output capacitor is dramatically reduced and its value finally drops to 200pF at 100V, which can be neglected. The value of the added ZVS capacitor became dominant and plays a role of controlling the MOSFET's dv/dt. Without C_{ZVS}, high dv/dt rate across the drain-source of MOSFET exceeds the dv/dt capability then the voltage Vgs may become higher than the threshold voltage, forcing the MOSFET into conduction and a catastrophic failure may occur. Selecting C_{ZVS}=3.3nF, the time for ZVS capacitor charging is: t_{ZVS}=205ns and the dv/dt rate is 2V/ns (maximum 15V authorized for selected MOSFET). Finally, the selected dead time td should be higher than the sum of tch and t_{ZVS}. The primary switching waveforms with td=400ns are reported by the following figure:



CH1: VQLgs, CH2: VQHgs, CH3: VQLds, CH4: Ir (50mV-1A)

Figure 2-25. Waveforms of ZVS switching with td=400ns at Vin=330V, P=300W

As reported from Figure 2-25, when Q_H is switched off, resonant current starts to discharge the C_{ossL} and charge the C_{ossH}. C_{ossH} performs a high capacitance value thus the charging is long, a hold-on time of about 100ns is detected. The voltage V_{QLds} across the MOSFET remains almost constant and the MOSFET Q_H is switched off at zero voltage. Then the half bridge middle point voltage decreases linearly. At the end of the dead time, the drain-source voltage decrease to zero, the MOSFET Q_L is then be switched on at zero voltage. At the primary side, both the ZVS switch-on and switch-off can be assured by carefully selecting the dead time length. However, ignoring the Vds voltage hold-on phenomena results in an early switch-on of MOSFET QL and result in hard switching. Figure 2.24 shows an experimental result with reduced td=200ns, executed at Vin=50V, open load. In order to protect the MOSFETs and boot-strap circuit, this experiment is implemented at a reduced input voltage level.



CH1: VQLgs, CH2: VQHgs, CH3: VQLds, CH4: Ir (50mV-1A)

Figure 2-26. Failure of a ZVS switching when td=200ns (tested at Vin=50V, no load)

As reported from the Figure 2-26, due to a limited dead time length and insufficient resonant current value, the voltage VQLds (Ch3) remain almost unchanged during the dead-time. Soft-switching is not attained and there is a great voltage fluctuation at MOSFET switch-on due to track's series parasite inductance and MOSFET paralleled ZVS capacitor. A large voltage spike appears with resonance which makes the converter work at hard switching.

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Chapter 3. Parallel-parallel Double Phase LLC: Operation and Control

3.1 Current Sharing in Double Phase LLC

3.1.1 Current sharing problems in phase-shift parallel-parallel LLC converter

In the previous chapter, it is described and proved that parallel interleaving two 1.25kW LLC power cells is a good solution for constructing a 2.5kW converter with high efficiency among a large output power range. The structure after power cell interleaving is shown in Figure 3-1.

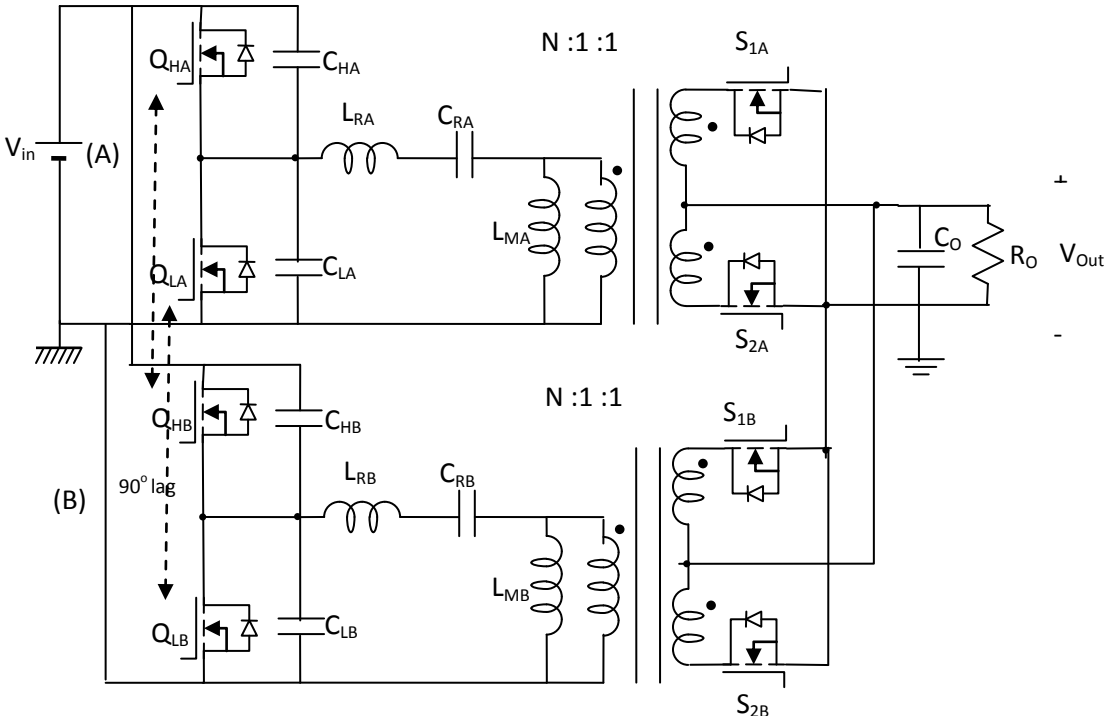


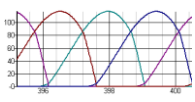
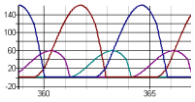
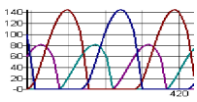
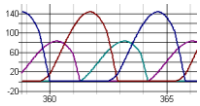
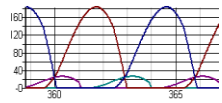
Figure 3-1. Two-phase interleaving LLC resonant converter with 90º phase shift

The double phase LLC resonant converter thus contains two phases LLC resonant cells, noted as cell (A) and cell (B), separately. To share the total output power, its input sides are connected in parallel and output sides are connected also in parallel. A filter capacitor C_O receives and filters the output current. The above double-phase or multi-phase LLC has appeared in several literatures [3-1 – 3-6] as a good candidate to manage high power applications. Traditional control method described in the above papers is to operate both the two phases at the same frequency with one same controller driver, but with a phase shift of

90° between adjacent cells to get an output current with fewer ripples. This works perfectly if the two resonant tanks of the two cells are identical. However, resonant cell component mismatch causes the two cells to exhibit different voltage conversion ratios characteristics; as a result, the load current is no longer equally distributed among the two power cells. Thus the applied control method is true only under the hypothesis that all the power cells have exactly the same electric parameters: the same resonant inductance, the same resonant capacitor, and the same magnetizing inductance. This is also to say, super-symmetry should be kept among both the power cells. If this is not the case, a slight component mismatch may introduce huge current balancing problems, more current attempts to pass through one of the power unit than the other, leaving the other units with lower power output. The following simulation is done to illustrate the current sharing problems under several typical component tolerances.

In the Simetrix software, set the power cell A as the reference power cell with the following resonant tank parameters: Lr= 7.5uH, Cr=50nF, Lm=42uH. The parallel-connected power cell B is considered to have value tolerances on these three tank components. The circuit operates at nominal power with the following electrical parameters are: Vin=360V, Ro=80mΩ, T=5.8us, f= 169.2 kHz, P=2.5kW. The primary driving signal of the power cell B is with 90º phase lag compared to the power cell A. Simulations are conducted in four scenarios: scenario No.1, the power cell B has 5% tolerance on resonant capacitor Cr (typical tolerance of a NPO ceramic capacitor); scenario No.2 : the power cell B has 10% tolerance on resonant inductor Lr (typical tolerance); scenario No.3 : the power cell B has 10% tolerance on magnetizing inductor Lm (typical tolerance); scenario No.4 : the power cell B has all the tolerances mentioned in the above three scenarios. The obtained results are shown in the following table.

Table 3-1. Current dissymmetry simulation results between two different power cells

Cell A	**Cell B**				
Reference Lr=7.5uH Lm=42uH Cr=50nF	Reference Lr=7.5uH Lm=42uH Cr=50nF	Scenario No. 1 Lr=7.5uH Lm=42uH Cr=52.5nF	Scenario No. 2 Lr=8.25uH Lm=42uH Cr=50nF	Scenario No. 3 Lr=7.5uH Lm=46.2uH Cr=50nF	Scenario No. 4 Lr=8.25uH Lm=46.2uH Cr=52.5nF
$I_B/(I_A+I_B)$	50%	26.9%	35.6%	37.2%	13.4%
Waveforms					

I_A stands for the average output current of the power cell A, while I_B stands for the average current of the power cell B. As is shown in the Table 3-1, component value tolerance has a great effect on the output power distribution, and may cause serious current sharing problems on the double-phase interleaved LLC power cell. Scenario 4 is a simulation of the current distribution under the worst case, where the current asymmetry problem is the most severe, from which the second power cell only shares 13.4% of the total power. As seen from the Table 3-1, the current sharing problem is more sensitive to the tolerance degree of the resonant capacitor Cr, as a 5% tolerance of Cr causes higher dissymmetry effect than 10% tolerance of Lr and Lm.

To better illustrate the current sharing result, Monte-Carlo analysis is executed in Simetrix software. Tolerance settings of 5% for resonant capacitors and 10% for inductors are taken in the simulation for both two power cells. Figure 3-2 shows the Monte-Carlo analysis results of the percentage shared by the power cell B versus the total output current, by executing 1000 steps of transient circuit simulation in Simetrix.

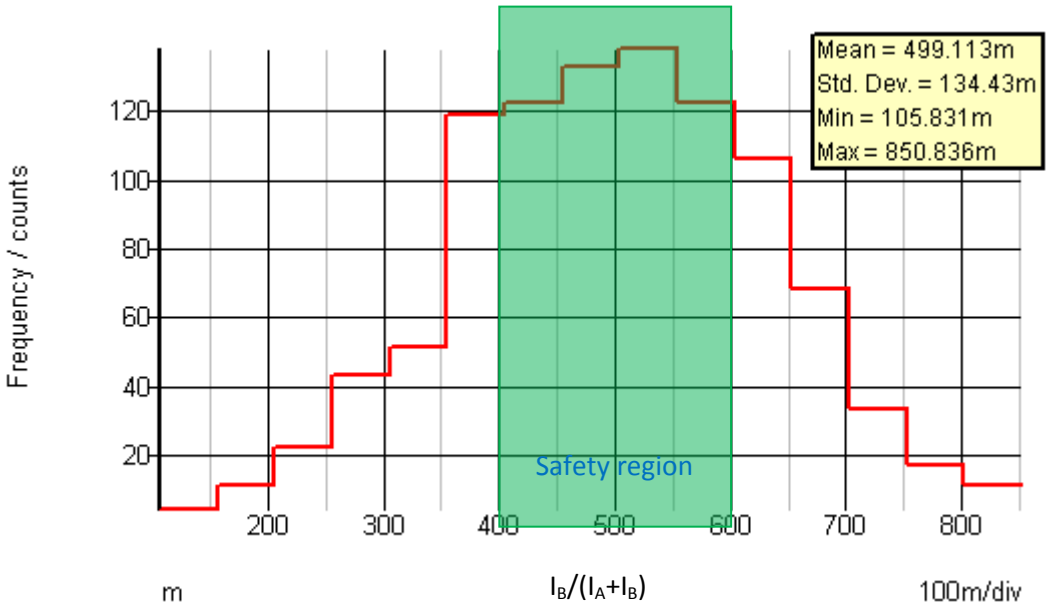


Figure 3-2. Histogram plot of the current percentage shared by the power cell B in Monte-Carlo analysis

$I_B/(I_A+I_B)$ with a variation of ±10% is accepted for keeping a relative balanced power distribution without causing serious operational problems at nominal power output. The Monte-Carlo analysis shows that the double-phase converter has a probability of 51.5%

working in the safety operation region, with a current sharing percentage limited into the interval [40%, 60%]. However, the converter still has a probability of 48.5% operating in the unbalanced current distribution region. In laboratory conditions, it is possible to assure a satisfactory current sharing by carefully selecting and identifying the component values before prototype assembly. However, in the automobile industry, the situation is not the same. Nearly 50% converter prototype will encounter current sharing problem and will be failed products.

In conclusion, from the simulation results, the well-applied unique operational frequency with phase-shift control method applied to double phase LLC converter is totally difficult to assure an equal current balancing between different power units, especially for DCDC converters in automobile industries where each resonant component is susceptible to have a value tolerance.

3.1.2 Current balancing among different power cells

Considering the phenomena of current dissymmetry existed in parallel-parallel interleaving LLC converter with phase-shift control, methods for current balancing among different power cells should be taken into consideration when designing the double phase LLC resonant converter. In [3-7] and [3-8], the authors analyzed the current balancing problems and gave some suggestions for designers to avoid serious current dissymmetry by careful circuit dimensioning. What the authors proposed are methods for ameliorating the current distribution under phase shift control method but it cannot overcome current dissymmetrical problems essentially. In [3-9], the author proposed to control the current sharing by controlling phase difference between adjacent power cells in a star connected three-phase LLC converter. All the three power cells operate at the same frequency but with variable phase differences to reduce the current mismatch. This control method applies very well at a three phase star connected LLC converter but the feasibility on double phase LLC is unknown.

In order to satisfy the equal current balancing requirements in double phase parallel-parallel LLC resonant converter, a novel control circuit is proposed in this thesis, which is a European patent of this dissertation [3-10]. The novel control method adopts two regulation loops: external output voltage loop and internal input current loop. It assures a current balancing among different paralleled power cells by controlling each cell's input current. In order to sense the input current of each power cell, a resistive shunt is connected in series with it. Figure 3-3 shows the proposed double-phase resonant converter with primary input current

sensors R_A and R_B. The sensor's resistance may vary between several mΩ and several hundreds mΩ, depending on the input current value and the sensor voltage level. In this project, considering the input current level, a shunt of 10mΩ is adopted. The shunt may dissipate up to 0.5W thus a large package of "1812" is selected. The current sensor is placed between the half bridge power cell and the primary power ground thus the current measurement is not floated.

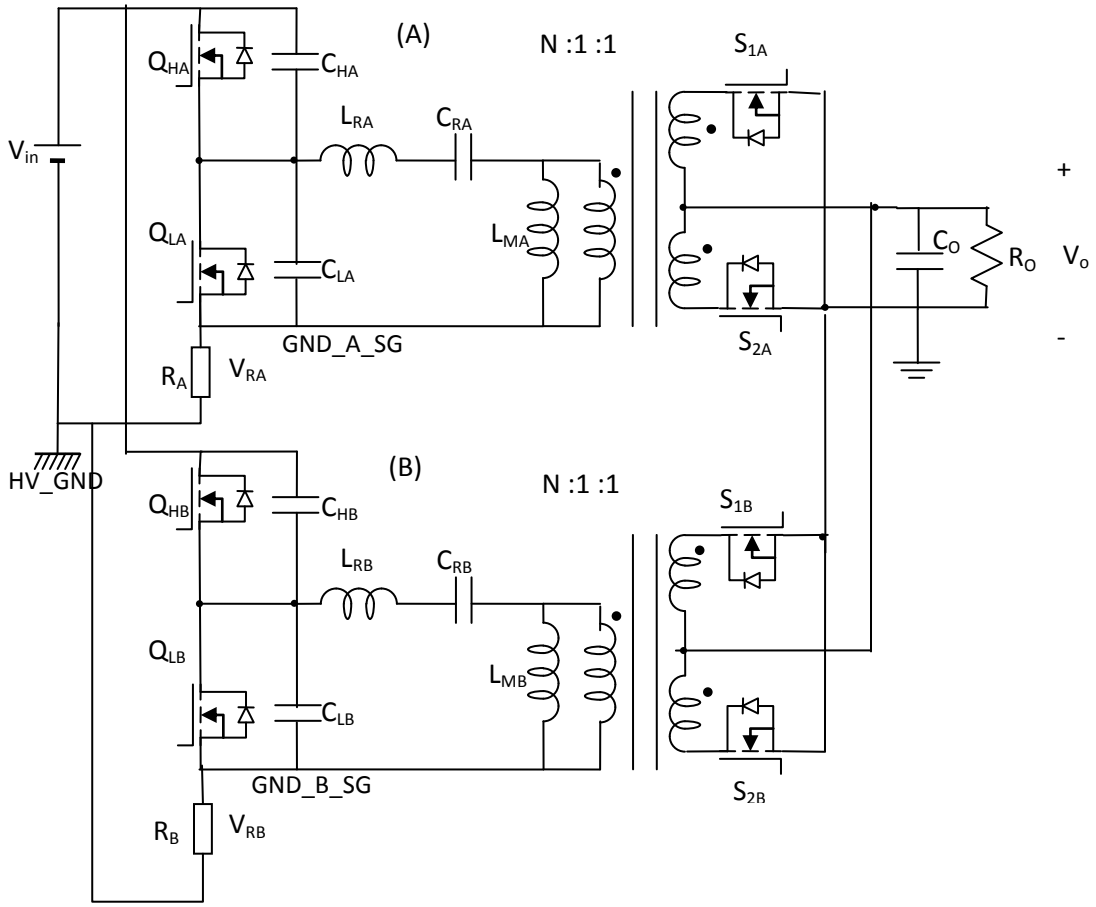


Figure 3-3. Proposed double phase LLC resonant converter with primary current sensors

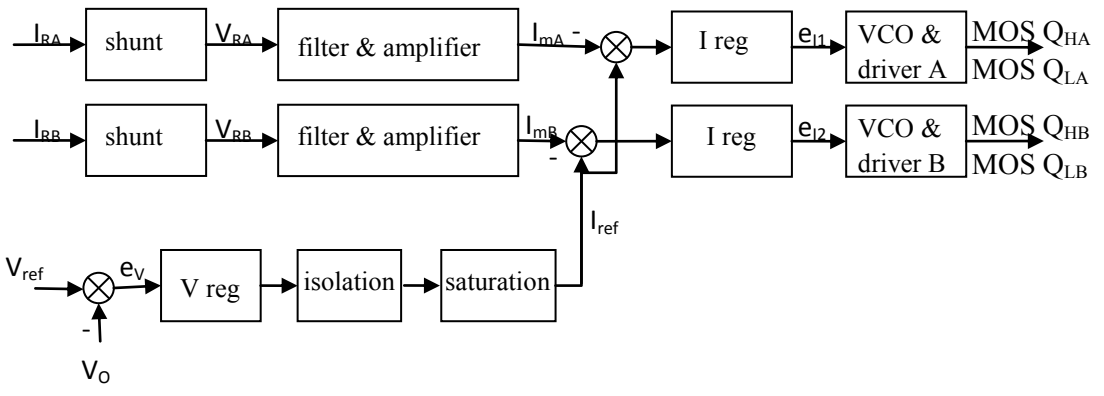


Figure 3-4. Bloc schematic of the control circuit for input current balancing applied to double phase LLC converter

The bloc schematic of proposed novel control circuit for input current balancing adapted to the double phase LLC converter is depicted in Figure 3-4. As shown in Figure 3-4, the current shunt R_A of the power cell A and R_B of the power cell B forwards the sensed input current signals in forms of V_{RA} and V_{RB}, separately. The sensed signals are filtered and amplified to a suitable level (noted as I_{mA} and I_{mB}) and they reflect the average active input current of each cell. The filter performs low pass characteristics and a high attenuation among the converter's operational frequency range to filter the AC noise brought by MOSFET switching. The whole control loop contains an external voltage control loop and an internal current control loop. The output voltage is compared with the reference voltage and the comparison error e_V is regulated by a voltage regulator PI. The voltage regulation gives a unique current reference I_{ref} for both the two power cells. This I_{ref} should be isolated from LV part and limited to a certain value to avoid over-current problems. The measured currents I_{mA} and I_{mB} are regulated to I_{ref} by its respective current regulators, while a uniform input current balancing among different power cells can be assured. The obtained comparison errors e_{I1} and e_{I2} are sent to different oscillators (can be either voltage controlled oscillator: VCO or current controlled oscillator: ICO) and drivers to drive the half bridge MOSFETs. It is apparent that under component mismatch, two converters operate at different frequencies to keep the same voltage conversion ratio. The operational difference nature of these two control strategies can be explained essentially by the voltage conversion ratio plotted in Figure 3-5 and Figure 3-6. Figure 3-5 shows an example of operational point movement with power cell component mismatch at nominal power under phase-shift control strategy. Figure 3-6 is an example of operational frequency differences under power cell component mismatch at nominal power under proposed double loop control. The cell A adopts the calculated tank parameters with Lr=7.5µF, Lm=42µF, Cr=50nF; the cell B adopts 10% capacitor tolerance with Lr=7.5µF, Lm=42µF, Cr=45nF. (Note: 10% maybe not a rational tolerance value for real applications. It is adopted as an example to better illustrate the current dissymmetry phenomena.)

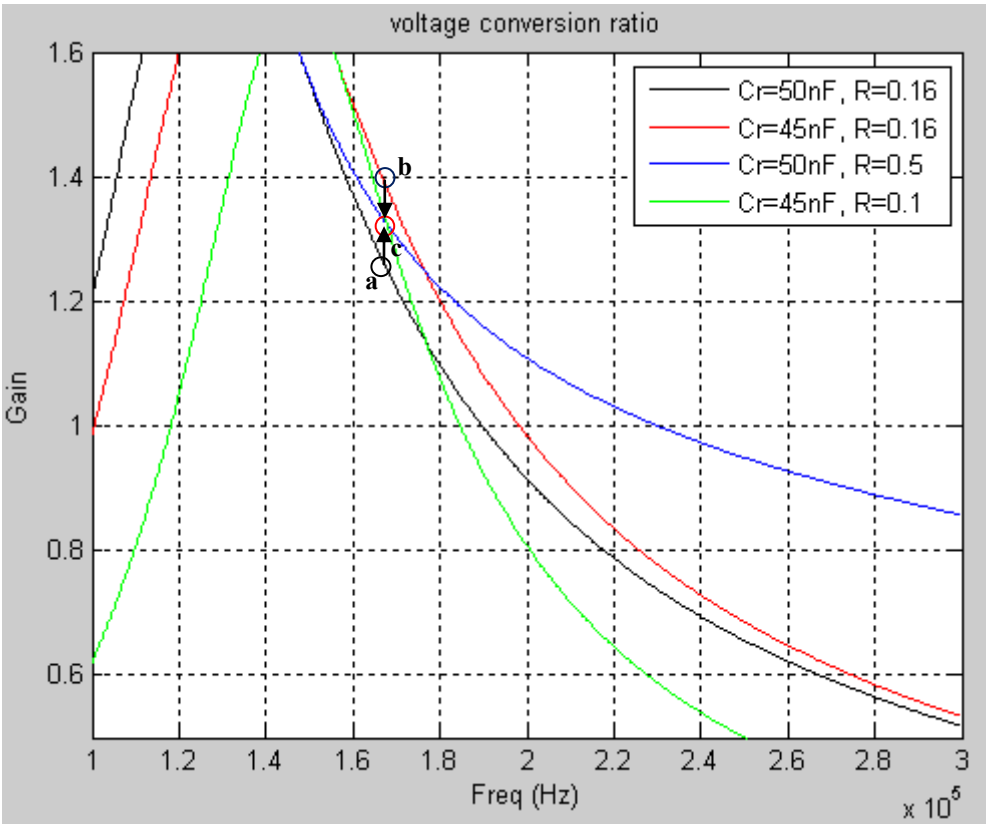


Figure 3-5. Operational point movement with component mismatch at Vin=360V, Vo=14V, P=1250W under phase shift control

The given input voltage and output voltage imposes a power cell gain of 1.3 required for both the two cells. If the output current is equally distributed between the two cells, the cell A operates at the point “a” with a gain less than 1.3 and the cell B operates at the point “b” with a gain more than 1.3. With parallel connection, both the two power cells should perform the same gain as they share the same input/output voltage at the same operational frequency of 169 kHz. Thus the cell A tends to share less load to increase its voltage conversion ratio and the cell B turns to share more load to decrease its voltage ratio. The operational point of cell A shift from “a” to “c” (with gain curve shift from black line to blue line) and the operational point of cell B shift from “b” to “c” (with gain curve shift from red line to green line). The system then stabilizes and voltage conversion ratios of both the two power cells are equal to 1.3. The cell A’s load resistance is increased to 0.5Ω and the cell B’s load resistance is decreased to 0.1Ω, which causes a current dissymmetry of IA/IA+IB=16.7%.

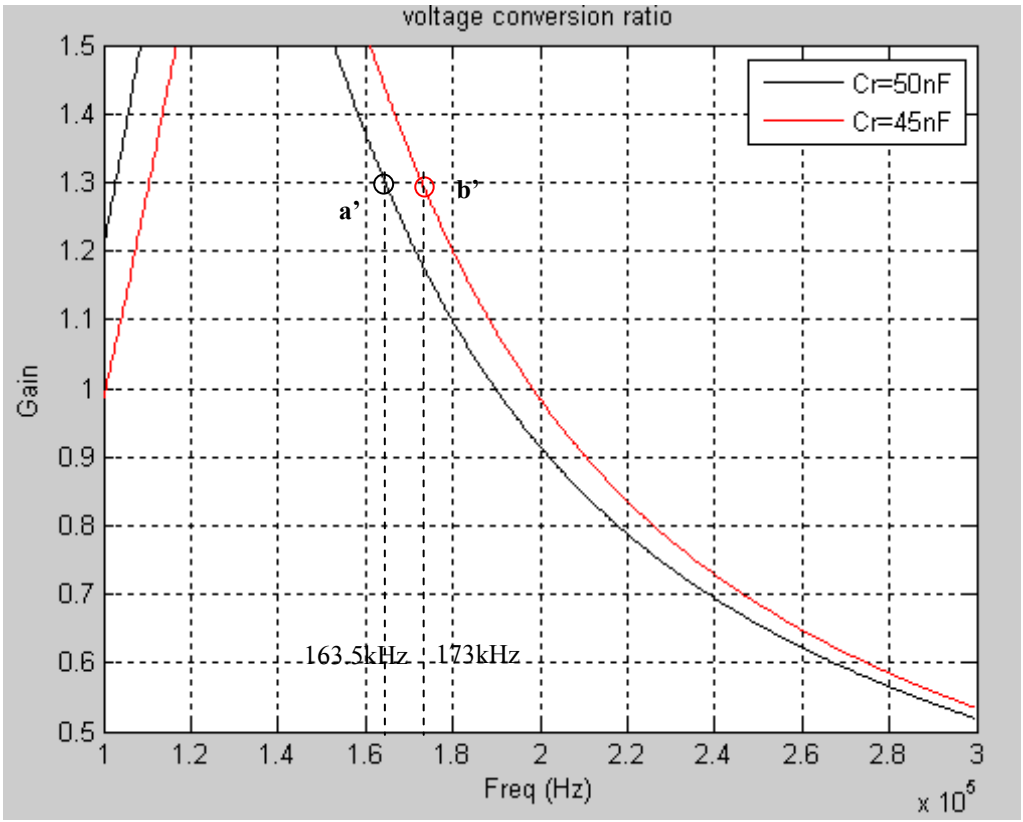


Figure 3-6. Operational points determination for two phase parallel LLC with component mismatch at Vin=360V, Vo=14V, P=1250W under proposed double loop control

As reported in Figure 3-6, using proposed double loop control, the case is not the same. Other than varying its load to adapt to the same voltage conversion ratio, the power cell varies its switching frequency to attain the same target. With double phase control loop and different drivers for different power cells, the switching frequencies for the two cells are not forced to be the same but to be independent of each other. Referring to Figure 3-6, the power cell A operates at 163.5kHz and power cell B operates at 173kHz. Each cell shares a load resistance of 0.16Ω and there is no current sharing problem in this control strategy.

It has to be reminded that although the proposed control strategy is applied to double phase LLC resonant converters, but the principle can be easily promoted to N phase (N>=2) LLC resonant converters by adjusting the number of current control loops.

In summary, the explications above show that the double-cell LLC converter by the proposed control strategy has the following features: 1) Simple to construct and execute. 2) Ideal current balancing among different power units regardless of the components value tolerance. 3) Uniform power distribution between different power units, thus uniform power loss and temperature rise. 4) Possible to handle higher power by paralleling more power units with

high efficiency. 5) When prompted to the operating between 2 voltage sources at a real vehicle, the internal current loop control simplifies converter power management during various operating mode. All the above features show that it is an excellent candidate for voltage regulation and current balancing of high power conversion in electric vehicle applications.

Based on the above discussions, the control board is designed as follows:

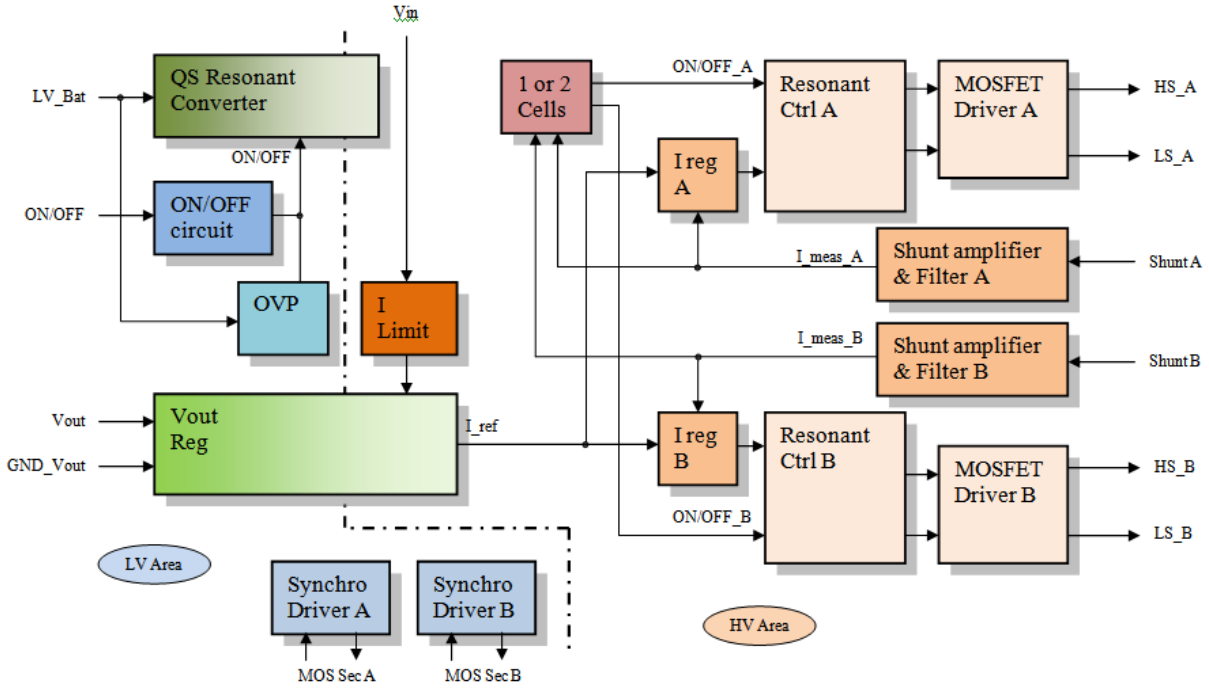


Figure 3-7.Framework of the control board applying proposed control strategy

A 6W quasi-resonant Flyback converter with multiple outputs is designed for providing 15V and 11V power supply to the high-side resonant controllers (+15V) and MOSFET drivers (+11V). This quasi-resonant Flyback converter converts the low side battery voltage (10~20V) to constant voltages with galvanic isolation. The designed converter is a Flyback converter with ZVS switching, while ZVS is realized by adding resonant capacitors and logic circuits to detect the zero crossing instant of MOSFET's drain-source voltage and it operates with a variable frequency between 100kHz and 300kHz with a maximum efficiency of 86%. The ON/OFF enables the Flyback converter to operate when receiving an ON command, and disables its operation when an over voltage (>18V) at LV_Bat occurs. An over voltage protection (OVP) circuit is designed to detect the over voltage at the LV battery. The output voltage is regulated by an output regulator and gives a reference signal *I_ref* for current regulation. The *I_ref* is isolated from the LV area and limited by the block 'I Limit' in

function of the input power and input voltage. The shunt amplifier & filter of respective power cell senses the input current of each power cell and the measured results are added and analyzed by '1 or 2 cells' to decide the number and order of cells to operate, following the logic indicated at Figure 2-2. The measured current of each cell is referenced to *I_ref* and regulated by its respective current regulators. A resonant controller is adopted at each phase for frequency conversion and drivers are utilized to amplify the driving capability. In addition, the adopted resonant controller FAN7631 is also possible to execute soft-start, over-current protection and under-voltage lock-out. The components arrangement at the control PCB card is shown in the following figure:

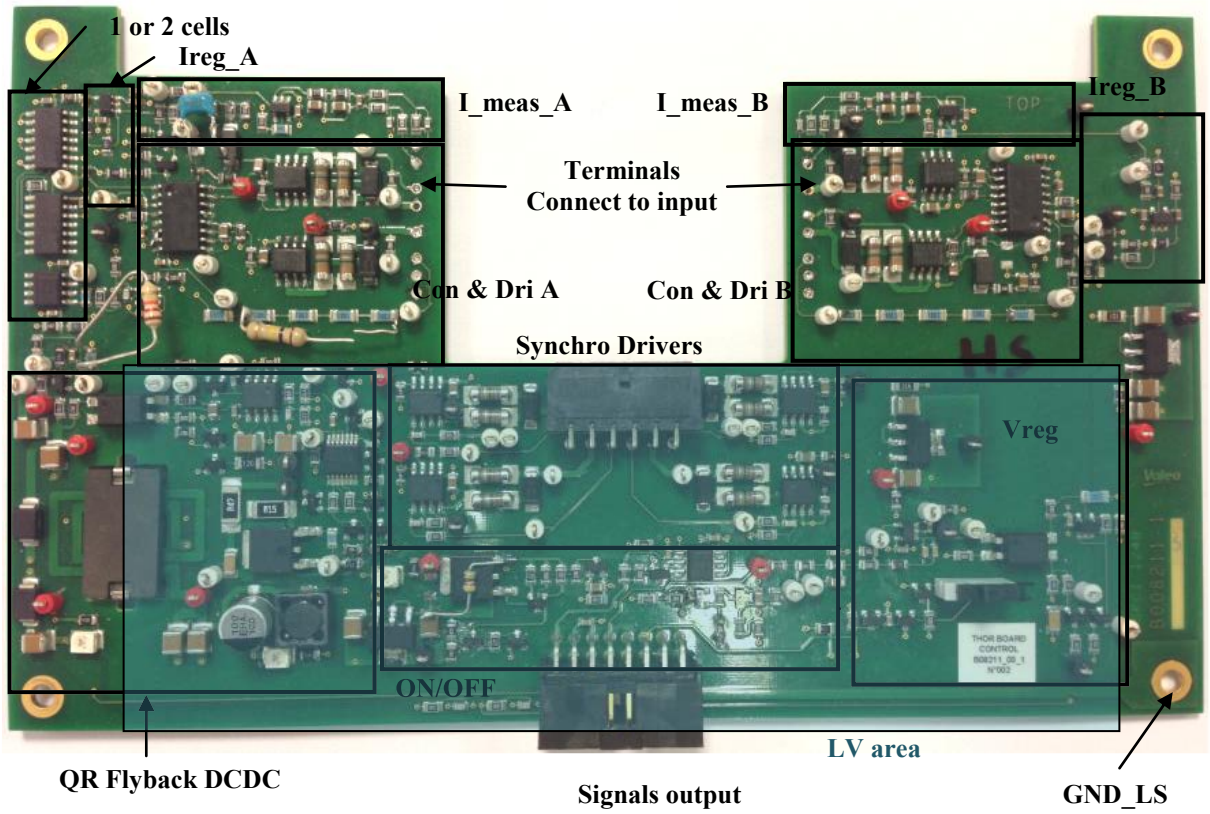


Figure 3-8. Components arrangement and design results of the control PCB card

The control board PCB adopts 8 layers, with 105μm thickness at the external layers and 70μm at the internal layers. The total PCB thickness is 1.6mm. As shown in Figure 3-8, an insulation distance of 4mm is used to separate the LV area (shadowed) from HV area. The ON/OFF, synchronous rectifier drivers and Vreg are placed at the LV area. QR Flyback converter is an interface between HV and LV area. The designed PCB board adopts a symmetrical structure, arranging the controllers and drivers of cell A at the left side and those of cell B at the right side. Wires are soldered at the pins and to drive the high side MOSFETs

which are located at the 'input filter' PCB board. The current measurement is placed close to the current regulation. The detailed electrical schematic can be found at the Annex1.

3.2 Control and regulations

In DC/DC power converters, the small signal analysis is essential for the feedback loop design. As to PWM power converters, the state space average modeling is a widely adopted solution, which groups the separate operating states proportionally by their respective duty cycle. This method provides simple but accurate solution for circuit's modeling for up to half switching frequency. However, in resonant converters, the state space average method can no longer be applied. In resonant converter, the switching frequency is too close to the resonant frequency of the resonant tanks and the state contain mainly switching frequency harmonics instead of low frequency content as in PWM converter, the circuit's dynamics cannot be precisely predicted. Two methods have been proposed to perform its small signal analysis: the extended describing function analysis [3-11~3-13] and time domain simulation method [3-14]. However, these methods are time-consuming and not easy to implement. The paper [3-15] gives some natural explanations of the LLC's v_{out}/f transfer function and gives some design considerations. As described in paper [3-15], the v_{out}/f is proportional to the slope of the voltage gain curve at the operating point; the poles moved with the operating point. The papers [3-16~3-19] also propose some other control method for stabilizing the LLC converter's control loop, for example, nonlinear adaptive control, etc. Other than the voltage single loop controls appeared at the above literatures, a double loop control scheme is established in this thesis, where the main difficulty lies in how to obtain the LLC's small signal transfer function of input current/switching frequency, noted as v_R/f (v_R is the voltage at the input current sensor). To simplify the modeling process, the Simplis software is adopted as an analyzing tool and the v_R/f transfer function analysis can be derived without repeated time domain simulation. With this software, bode diagram of the converter's transfer function at given operating point can be simulated in several seconds instead of several hours in previous time domain simulation method. Based on the obtained transfer function diagrams at the current open loop and voltage open loop, different control scheme are proposed and regulators are designed to regulate the input current and output voltage dynamics. Finally, the simulation results are provided to verify the stability and dynamic performance of the designed LLC resonant converter.

The Simplis software has integrated a Periodic Operating Point (POP) Analysis which adopts a special algorithm to accelerate convergence to the steady-state for a switching system, thus

the converter can reach the steady state faster than it would be in other simulation methods. The POP analysis is realized by different iterative time domain simulations. After reaching steady state, by injecting AC excitations at the desired point, the software executes an AC sweep analysis at a given frequency range to get the transfer function of any two points set as input and output. Through this simulation, the transfer function of LLC converter can be simulated by correctly imposing its steady operational point, without establishing its small signal model. The detailed simulation results are discussed in the following parts.

3.2.1 Current regulation control

As shown in Figure 3-3, input current of each power cell is measured by its respective shunts R_A and R_B, and the result is a voltage difference between the power ground and the signal ground, noted as HV_GND, GND_A_SG for the cell A and GND_B_SG for the cell B, respectively. The following figure show the input current filtering and amplifier circuit for the power cell B. The circuit at power cell A is the same as that in power cell B.

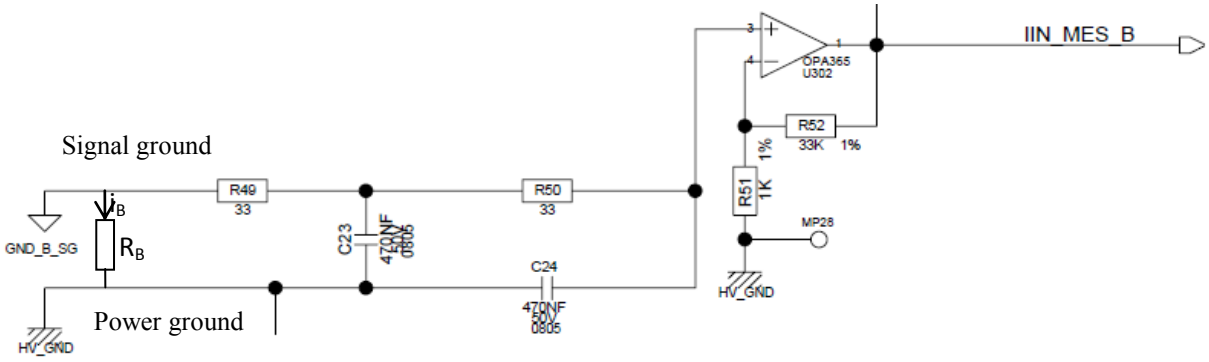


Figure 3-9. Input current filtering and amplifier circuit at the cell B

The input current is sensed by a 10mΩ resistive shunt inserted between HV_GND and GND_B_SG, with a maximum average input current of 4.2A (42mV maximal). Then a second order RC low pass filter is adopted to extract the average input current; its transfer function is written as $G_{LPF}(s)$. The signal is then amplified by U302 with a gain of G_A=34 for further processing.

$$G_{LPF}(s) \approx \frac{1}{(1+sC_{23}R_{49})^2} \quad (3-1)$$

The proposed input current regulation circuit is shown in the following figure:

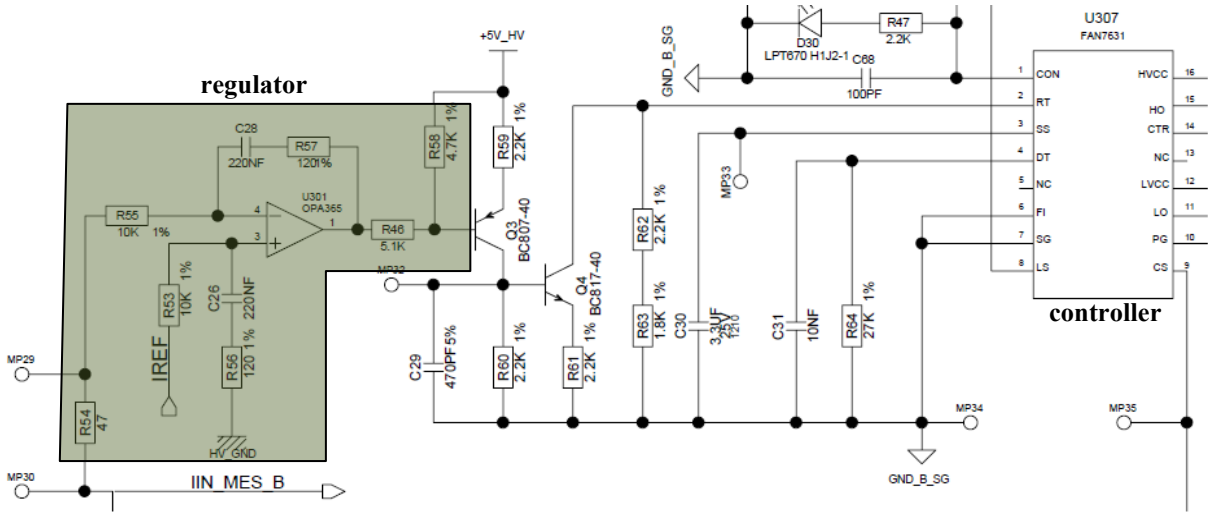


Figure 3-10. Current regulation circuit applied for the power cell B

The controller FAN7631 integrates a current controlled oscillator (ICO) where the frequency is proportional to the current sensed at the pin RT of controller U307(internally regulated to +2V), with a gain of 270Meg.

$$f = 270Meg.I_{RT} \quad (3-2)$$

The resistances R62 and R63 set a minimum current of 0.5mA at the pin RT, which impose a minimum switching frequency of 135 kHz. The switching frequency increases as the current flowing through R61 increases. The switching frequency can be regulated indirectly by the base voltage at Q4, through varying the total current sensed at the pin RT. The transistor Q3 operates at its forward-active region and the current flowing through R59 and R60 is the same. The following equation can then be obtained:

$$V_{Q4b} = 5V - V_{Q3b} - V_{be} \, (3-3)$$

Here, the transistor Q3 plays two roles: Firstly, the resonant controller is referenced to GND_B_SG and the regulator is reference to the GND_HV. Q3 transfers the regulator's output voltage to the controller side by current equilibration through Q3's collector and emitter, thus resulting in insulation between the two grounds. Secondly, since the voltage conversion gain is decreasing with the increasing of frequency, increase the voltage VQ4b decreases the frequency and increases the cell's input current. In order to realize a negative feedback, the gain is inversed by the transistor Q3, with the following equation obtained from (3-3):

$$\tilde{v}_{Q4b} = -\tilde{v}_{Q3b} \ (3-4)$$

The voltage V_{Q3b} controls the current flowing through R61 thus controls the operational frequency, in a way of negative feedback.

A resistance R46 is placed at the regulator's output. This resistance also has two roles. Firstly, the resistance avoids the possible saturation of the PNP transistor Q3 at the start phase. Without this resistor, once the output of U301 gives 0, the Q3 conduct and VQ3e=VQ3c>VQ3b, which saturates definitively the transistor Q3. With this resistor R46, Q3 will never be saturated even if the output of U301 gives 0. Secondly, this resistor limits the maximal switching frequency by limiting the maximum voltage of VQ4b. In case of U301 gives 0, the VQ4b attains its maximum value of 1.9V, which signifies a maximum current of 0.59mA flowing through R61 (signifies a maximum possible switching frequency of 290 kHz). However, this resistance also influences the gain of the control loop and reduces the regulator's gain with:

$$G_r = \frac{R_{58}}{R_{46} + R_{58}} \ (3-5)$$

The block diagram of current regulation for cell B can be represented in the following figure:

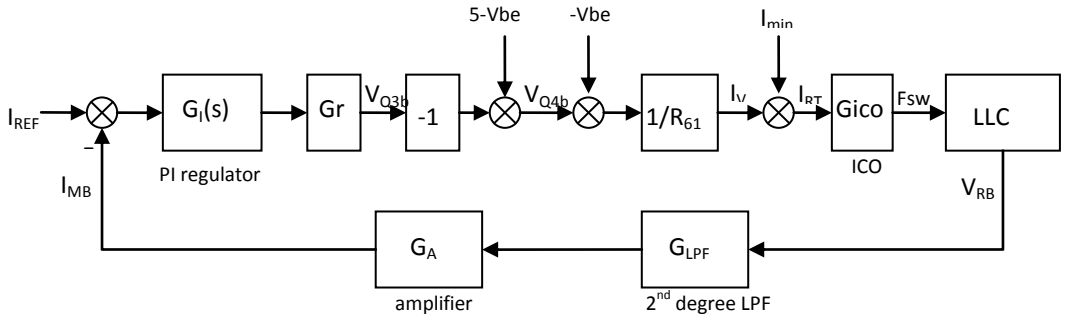


Figure 3-11. Block diagram of current regulation in proposed LLC resonant converter

The adopted PI regulator's transfer function can be expressed as follows:

$$G_I(s) = \frac{\tilde{u}_{301\_1}}{\tilde{\imath}_{REF} - \tilde{\imath}_{MES}} = \frac{R_{57}}{R_{55}}\left(1 + \frac{1}{sC_{28}R_{57}}\right) \ (3-6)$$

The current open loop transfer function before correction and after correction can be presented as follows:

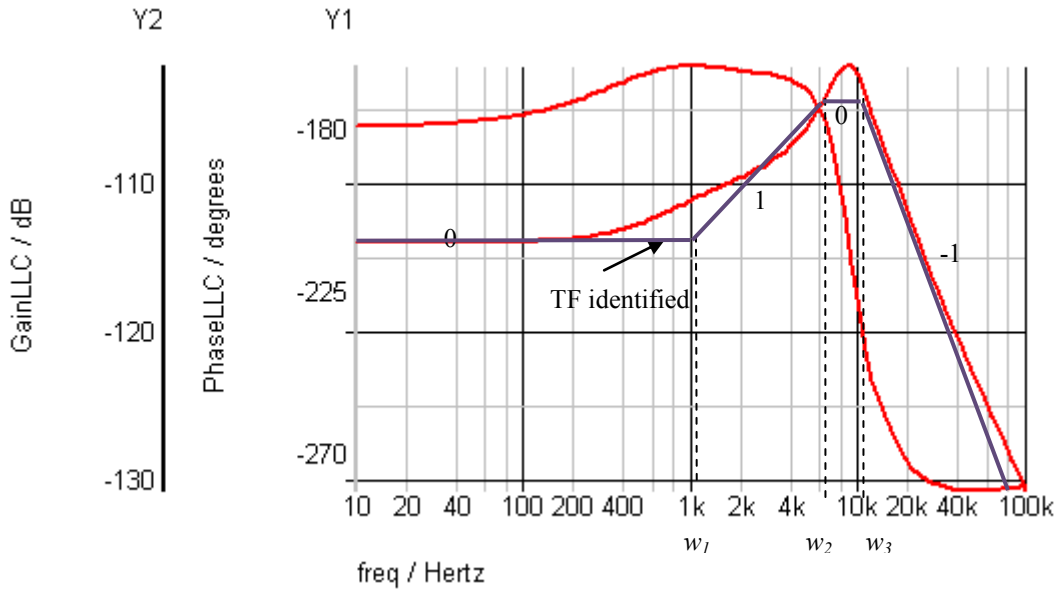
$$G_{BC}(s) = -\frac{G_A G_{ICO}}{R_{61}} G_{LPF}(s) G_{LLC}(s) \quad (3-7)$$

$$G_{AC}(s) = G_I(s) G_R G_{BC}(s) \quad (3-8)$$

The LLC power cell's input current to switching frequency transfer function $G_{LLC}(s)=v_R/f$ is unknown to us. A simple way to study its characteristic, as discussed in the above section, is to utilize Simplis software to plot its transfer function. The LLC circuit with the proposed current regulation circuit is modeled and simulated in Simplis software to obtain its transfer function, which is shown in the following Figure 3-12. As the frequency varies in kHz and sensed input current v_R varies in mV, the LLC's transfer function $G_{LLC}(s)=v_R/f$ has a very low gain. The phase of $G_{LLC}(s)$ starts with $-\pi$, which signifies a negative gain of $G_{LLC}(s)$. A resonance is detected at 10 kHz. The $G_{LLC}(s)$ approximation results by identification of transfer function's breakpoints can be expressed in the following form:

$$G_{LLC}(s) = -K \frac{1 + \frac{s}{\omega_1}}{\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)} \quad (3-9)$$

Through identification, K=2e-6, ω1=1kHz, ω2=6kHz, ω3=10kHz. ω2 is very close to ω3. In order to damp the resonance at ω3, the second order RC filter's breaking frequency is set to be ω3. The low pass filter $G_{LPF}(s)$ adds two supplementary poles at 10 kHz, of which the results are shown as in the following figure:



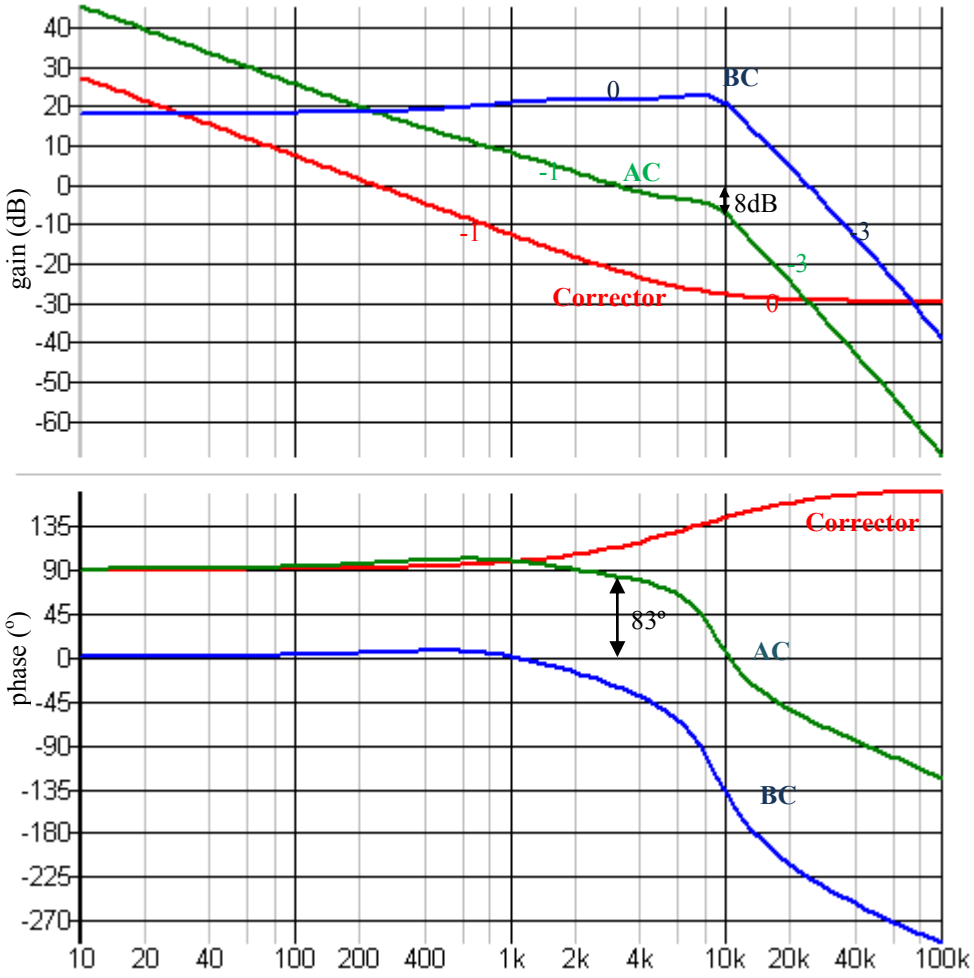


Figure 3-12. Bode diagram of $G_{LLC}(s)$, open loop transfer function before correction (BC) and after correction (AC) at nominal power 1250W, Vin=330V

It can be considered that, after low pass filter damping, the open loop transfer function before correction performs a 0 slope up to 10kHz and a -3 slope afterwards. Select the PI regulator's zero to compensate one of these three poles, and select a low gain to obtain a large phase margin, as shown in the above figure. After correction, the obtained bandwidth is 3kHz, with a phase margin of 83º and a gain margin of 8dB.

Increasing input voltage or decreasing load makes the input current less sensitive to the variation of switching frequency, thus the open loop gain BC shall be decreased. As a result, the condition of operating at nominal power with Vin=330V is a case where a highest open loop gain may occur, which is the most instable operating point to be considered when dimensioning regulator parameters. The following figure shows the bode diagram of open loop transfer function at light load Vin=330V, P=100W.

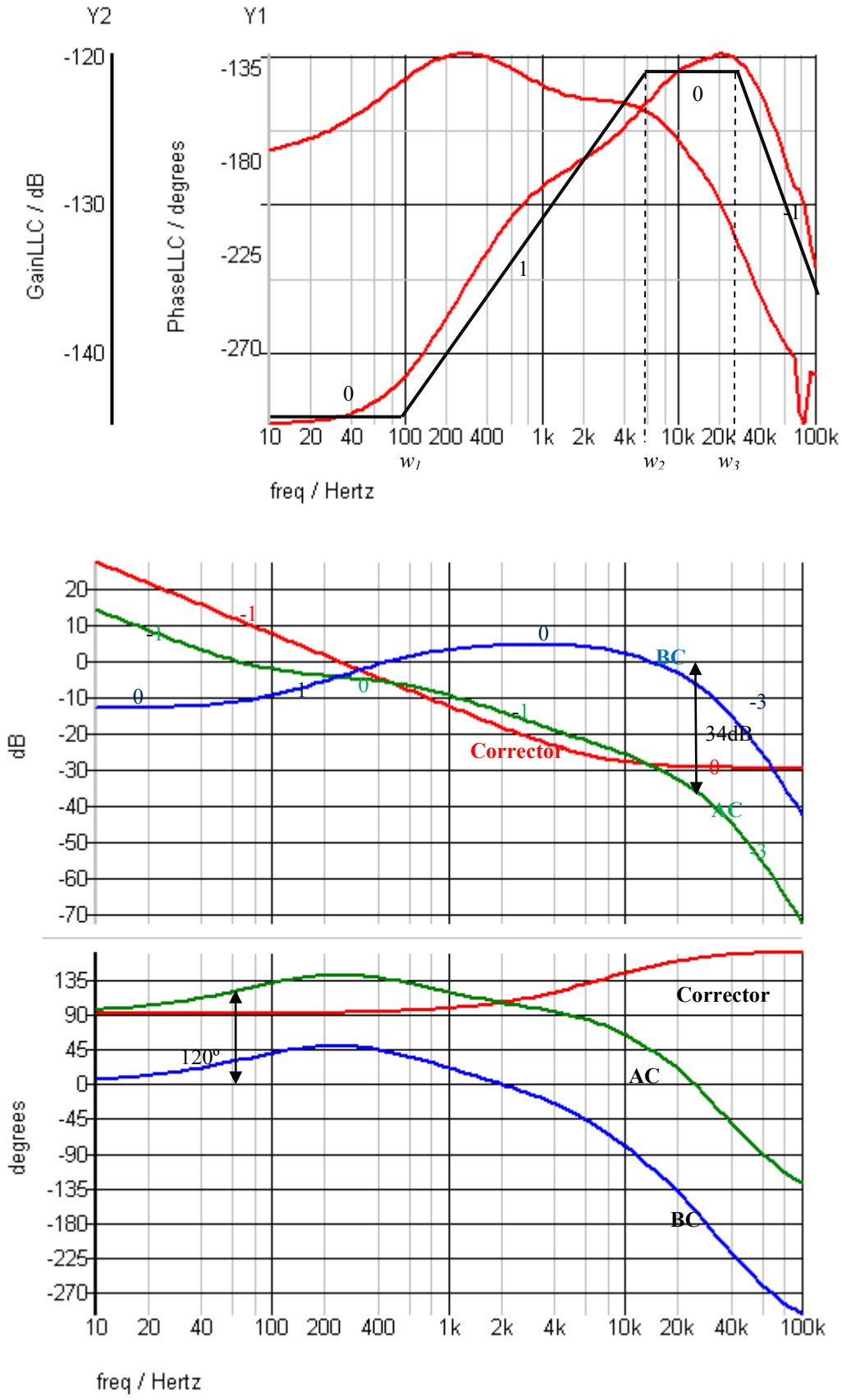


Figure 3-13. Bode diagram of open loop transfer function before correction (BC) and after correction (AC) at 100W, Vin=330V

As reported in the above figures, at Vin=330V P=100W, through identification, the parameters in transfer function $G_{LLC}(s)$ are: K=0.6e-7, ω1=100Hz, ω2=6kHz, ω3=25kHz. Due to the fact that the zero frequency ω1 is left sifted to 100kHz, the gain starts to increase at very low frequency and results in a large resonant gain at 10kHz, which cannot fully be damped by the inserted low pass filter. The transfer function before correction performs a 0→-1→0→-3 slope characteristic rather than 0→-3 characteristic. The regulated system's bandwidth is reduced to 60Hz, with a phase margin of 120º and a gain margin of 34dB.

3.2.2 Voltage regulation control

The electrical schema applied to voltage control is presented as follows.

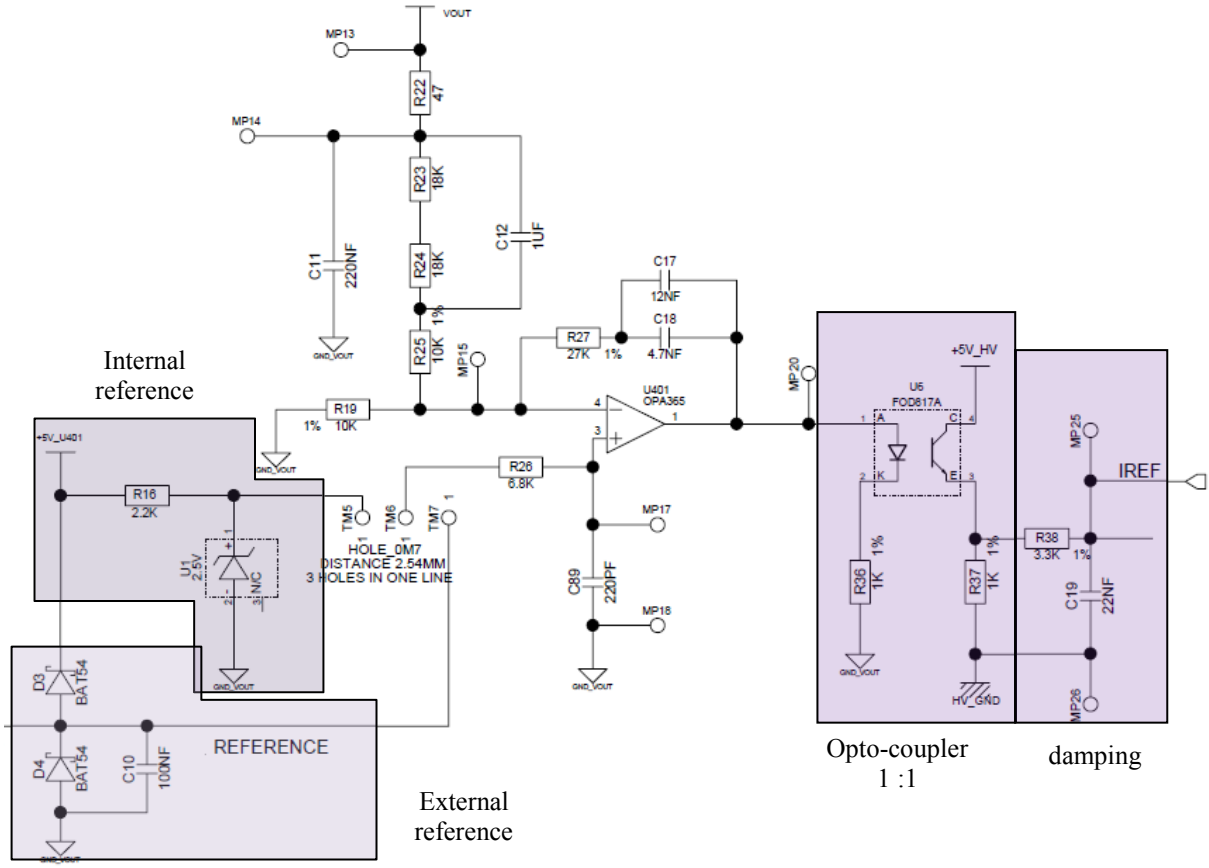


Figure 3-14. Electric schema for voltage regulation

The voltage reference signal may origins from an internal signal by U1 (reference 2.5V) or by an external signal. The internal signal regulates the LLC's output voltage to the nominal output voltage of 14V. A PI regulator is adopted for voltage regulation, with its transfer function represented as:

$$G_V(s) = \frac{\tilde{u}_{401\_1}}{\tilde{u}_{REF} - \tilde{u}_{out}} = \frac{R_{27}}{R_{25}}\left(1 + \frac{1}{s(C_{17} + C_{18})R_{27}}\right) \quad (3-7)$$

R22 and C11 form a low pass filter for filtering the high frequency voltage ripples at Vout. Opto-coupler U6 is used here for transforming the compared errors to LV side.

The LLC's voltage open loop transfer function is plotted by Simplis software and the results are shown in Figure 3-15. In order to obtain a more robust system with large bandwidth, a RC circuit is designed for damping the resonance found at LLC's voltage open loop transfer function.

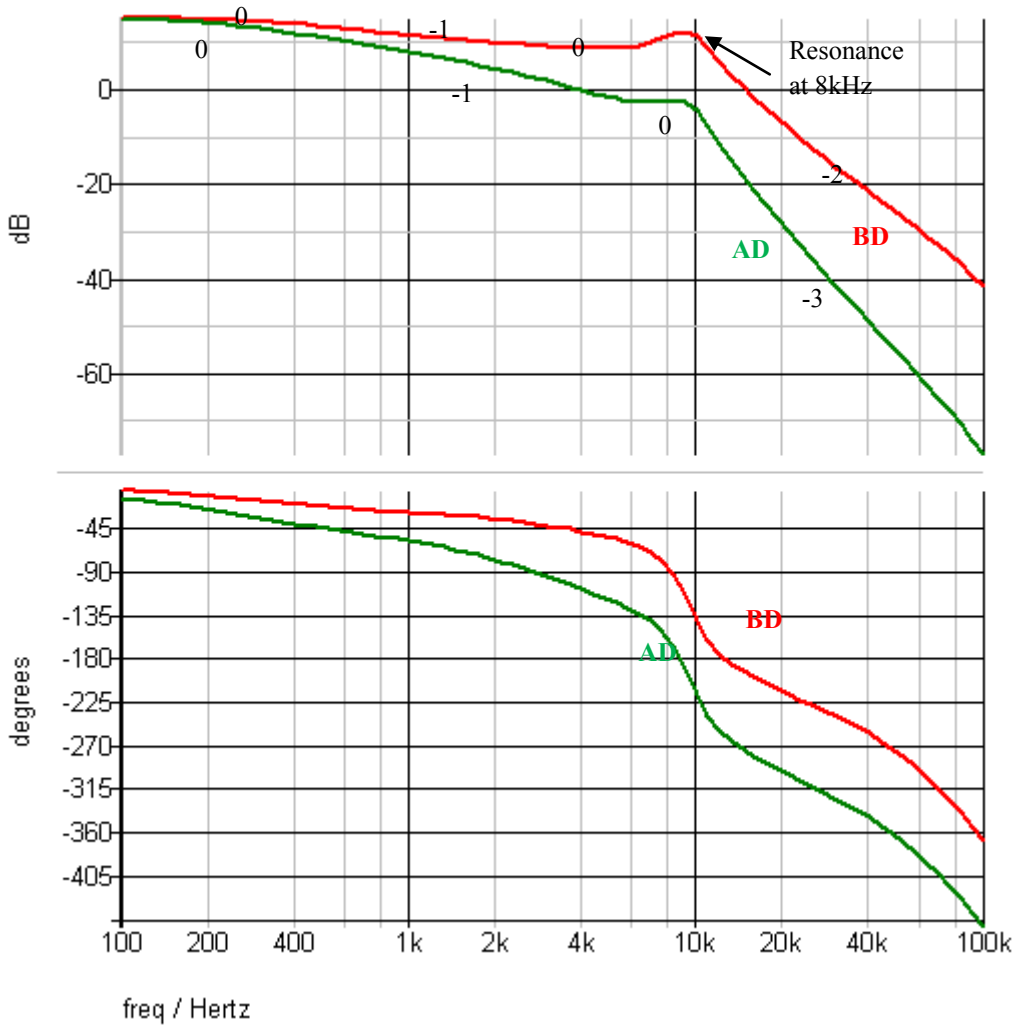


Figure 3-15. Bode diagram of LLC's voltage open loop transfer function before RC damping (BD) and after RC damping (AD)

As shown in Figure 3-15, without the RC damping, a resonance at 10kHz is detected, which adds the difficulties for designing the voltage regulator. Thus an RC damping (R38 C19) with a breaking frequency equal to the transfer function's zero point (2.5kHz) is thus introduced. After this RC damping, the zero is compensated and the gain at resonance point is greatly decreased, ready for regulation by a PI controller. It should be noted that adding a RC damping filter reduces also the phase-margin, thus the regulator's parameter should be correctly selected to satisfy the voltage loop stability requirements.

The proposed control diagram for voltage regulation can be represented at the following figure:

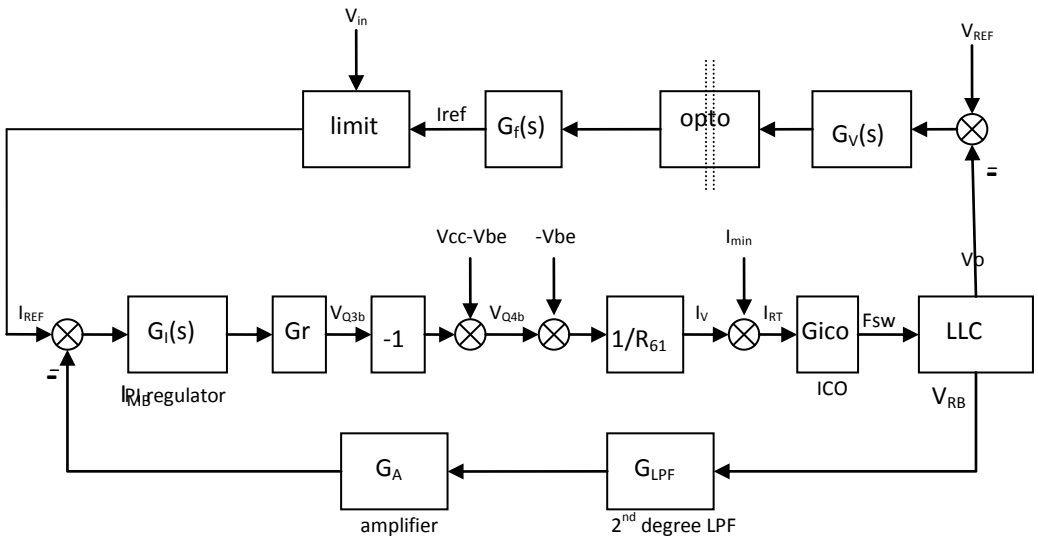


Figure 3-16. Block diagram of voltage regulation in proposed LLC resonant converter

As shown in Figure 3-16, $G_f(s)$ is the transfer function of the RC damping circuit and Gv(s) is the adopted voltage regulator. Opto-coupler has a constant unit gain. The Iref limit function limits the reference current to a certain value in function of the input voltage and does not interfere into the transfer function. In order to design the regulator parameters, Simplis software is utilized to plot the voltage open loop transfer function before correction. Figure 3-17 and Figure 3-18 shows the voltage open loop transfer function before or after correction under different operating points.

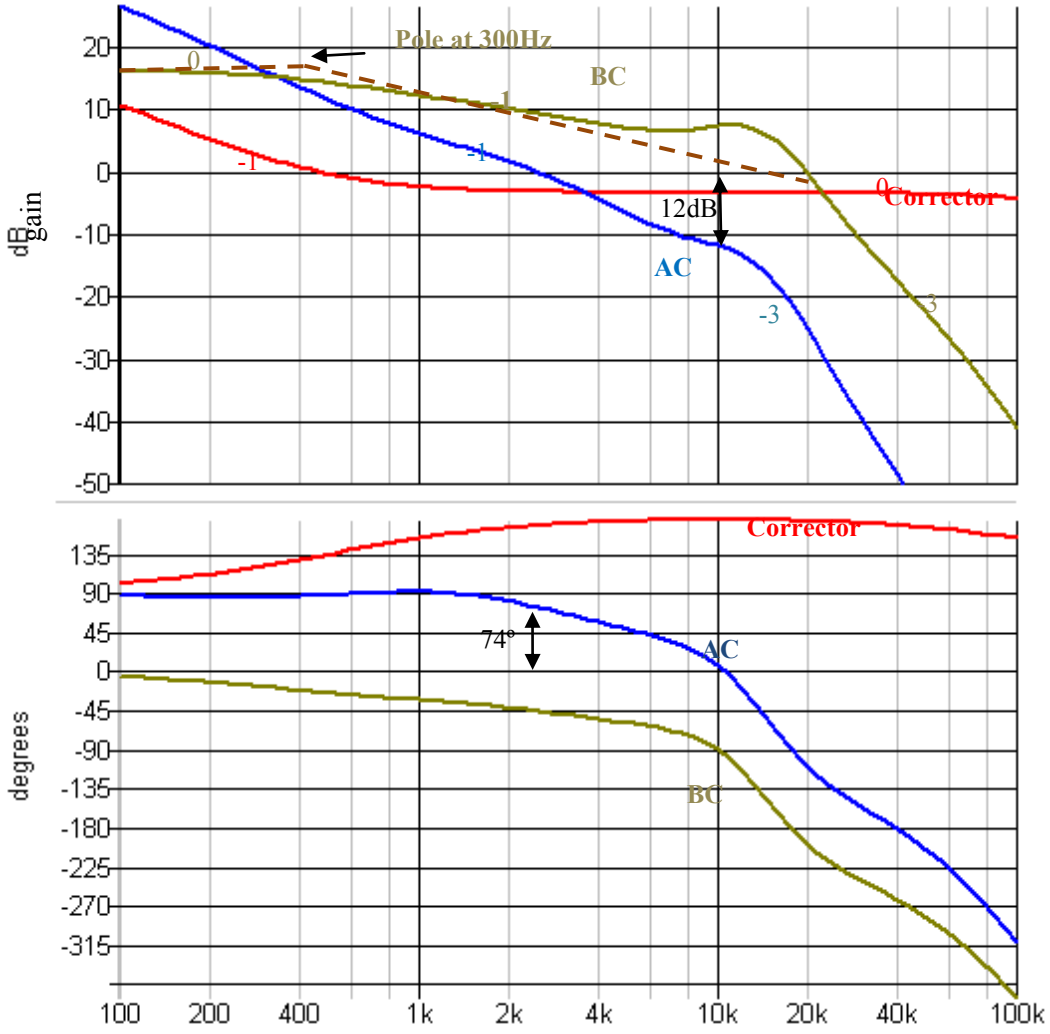


Figure 3-17. Bode diagram of voltage open loop transfer function before correction (BC) and after correction (AC) at nominal power 1250W, Vin=330V

As depicted in the above figure, the voltage open-loop transfer function BC can be approximated by a 0→-1→-3 curve, while the first pole appears at 300Hz and the second double pole appears at 20kHz. The corrector is designed with a high gain to increase the bandwidth and the zero is placed at 300Hz to compensate the voltage open loop transfer function's pole. After correction, the converter's bandwidth is 2.5kHz, with a phase margin 74º and a gain margin 12dB.

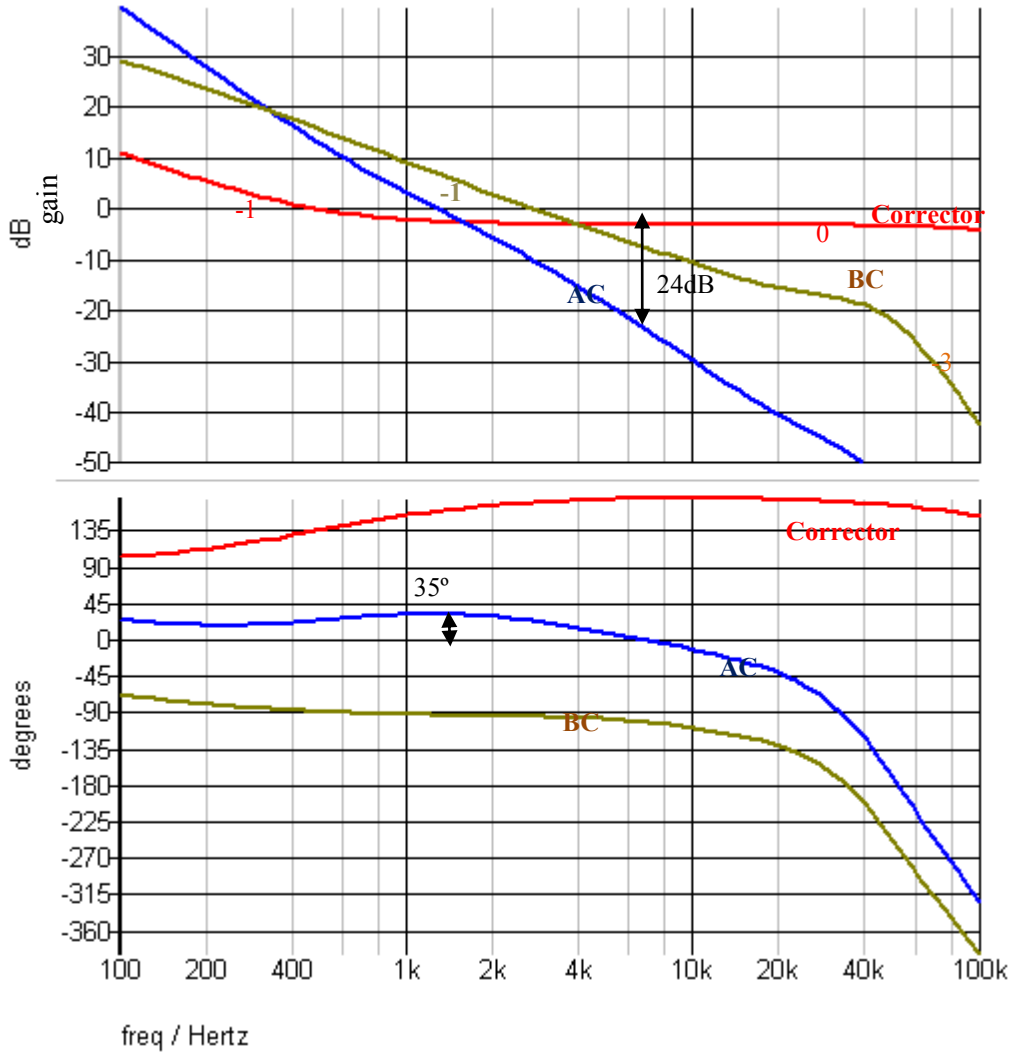


Figure 3-18. Bode diagram of voltage open loop transfer function before correction (BC) and after correction (AC) at power 100W, Vin=330V

From the results reported in Figure 3-18, at light load, the system's bandwidth is 2.6kHz, with a phase margin 35º and a gain margin 27dB.

It can be seen that both the regulator parameters are precisely designed to obtain a stable, rapid and precise current/voltage control.

A *Iref* limitation circuit is designed for limiting the current reference signal, forwarded by the voltage regulator, to a certain range to avoid over current problems. The circuit is designed as in the following schema Figure 3-19.

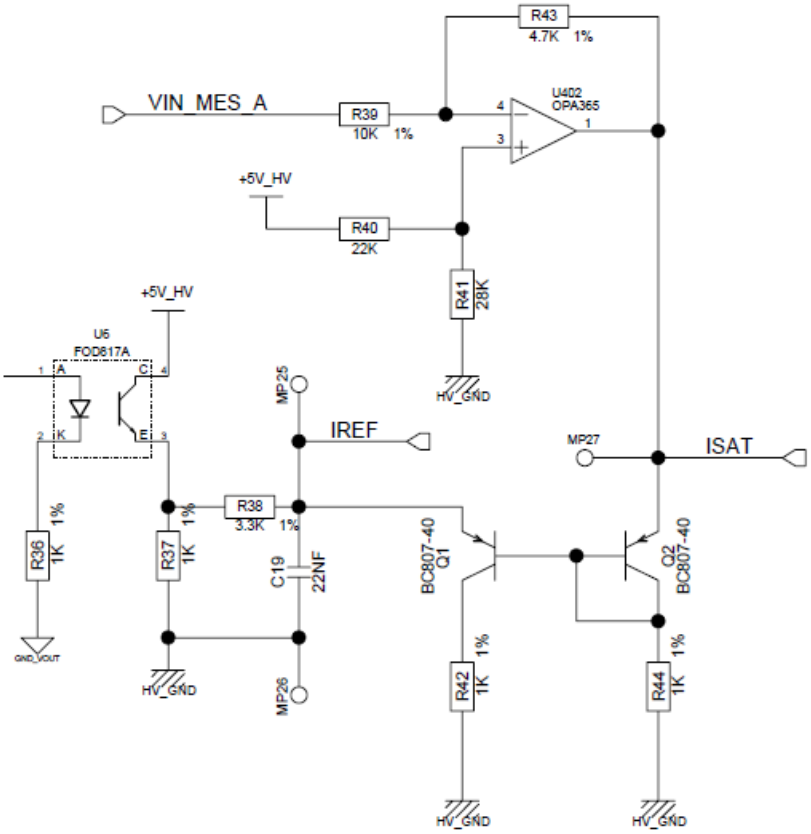


Figure 3-19. Iref saturation circuit design in voltage control loop

The aim of *Iref* limitation is to limit the total power of one cell to less than its maximum power thus the *Iref* signal should be limited to different values under different input voltages. According to the measured input voltage, the operational amplifier U402 forwards a signal ISAT, signifying the maximum current *Iref* to be limited. The I_{SAT} signal is linearly inverse proportional to the input voltage.

Referring to the Figure 3-19, Q2 is always active. In case *Iref* is higher than the I_{SAT}, Q1's base-emitter is forward biased and *Iref* is limited to VQ2b+Vbe. Since the base-emitter voltage of the two PNP transistors can be considered as the same, the Iref is limited to ISAT. The voltage difference is addedw at the resistance R38.

Iref limitation is a way for realizing over current protection. Especially when one cell encounters default at high output power, the input current of the other phase is limited to ISAT to avoid that all the power passes through this cell. This is a great advantage of this control method than phase shift double cell LLC. The converter is further protected by various current protections (to protect principally the HV and LV MOSFETs), including output

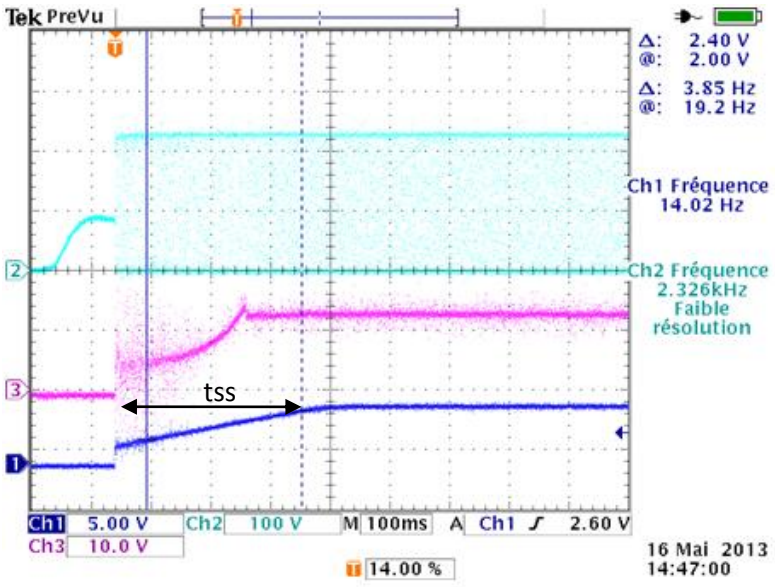
current protection, fast input current protection, which will be presented at the following section.

3.3 Other Controls and Protections

Other than current and voltage control loop, the LLC converter includes also soft-start control, over-current protection, over voltage protection, etc, to insure a complete system protection to abnormal conditions.

1) Soft-Start

Since the voltage conversion ratio of the resonant converter is inversely proportional to the switching frequency in ZVS mode, the soft-start is implemented by sweeping down the switching frequency from a high initial frequency (600 kHz) until the output voltage is established. The soft-start function is integrated into the controller FAN7631. Referring to the Figure 3-20, during soft-start, the sourcing current of the SS pin (30μA) charges the capacitor C30 and the voltage Vss rises slowly until it reaches the threshold (4.2V), allowing slow decrease of the switching frequency. The total soft-start time then can be parameterized by selecting the correct capacitance C30.



CH1: Vss (5V/div), CH2: VQLds (100V/div), CH3: Vo(10V/div)

Figure 3-20. Experimental results for converter's soft-start

The soft-start time is programmed to tss=300ms. As shown in Figure 3-20, the converter needs about 200ms to establish to the targeted output voltage and then the voltage regulation

takes part in. During soft-start, the output voltage is slowly increased until constant output is established.

2) Over current protection

During operation, the converter is subject to various over-current events. In order to protect the correct operation and avoid damages to the power components, over current protections are adopted at both primary and secondary sides.

At the output side, a 220A fuse is connected in series at the converter's output to avoid short-circuiting the LV battery in case of converter failure.

At the primary side, fast over current protection is realized by the CS pin of FAN7631. As shown in the Figure 3-10, the CS pin senses the instantaneous input current of each power cell by the added resistive shunt. When the sensed voltage on the CS pin (minus value) drops below the threshold V_{OLP} (-0.37V) for more than 200ns, FAN7631 disables the driver signal and repeats discharging and charging the Css four times, then restarts. This avoids the converter to suffer from temporary over-load without interrupting its normal operation.

Besides, if short-circuit happens at the secondary-side rectifier MOSFETs or at primary side components, a large current can flow through the primary MOSFETs. When the sensed voltage drops below -1.1V, the switching operation is disabled completely.

3) Over voltage protection

Over voltage at the LV battery side is considered at the development of this prototype. The supply voltage for all components at secondary LV side (including Flyback controllers, synchronous drivers and other components) origins from the LV battery voltage and is internal limited to +15V. In case the LV battery voltage is higher than 15V, a circuit is designed to internally limit the supplying voltage to +15V, shown as follows.

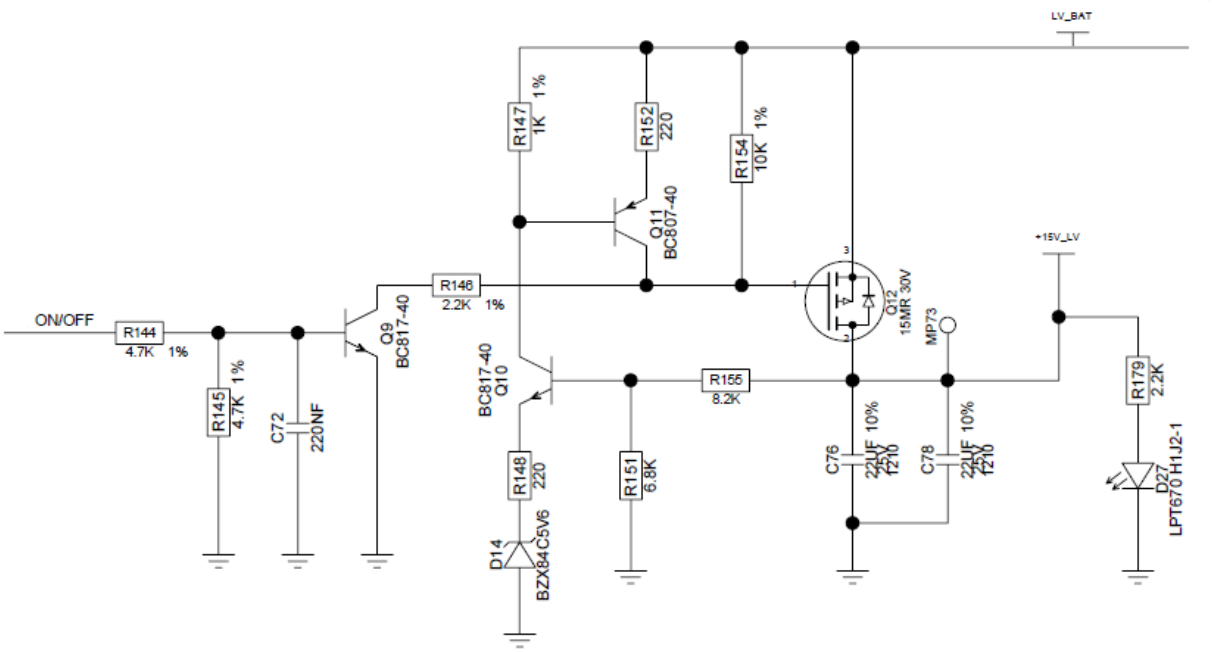


Figure 3-21. Voltage limitation circuit limiting the LV supply voltage to 15V maximal

The operation is presented in the following two cases:

a. LV_BAT is lower than 15V. When On/OFF gives ON, Q9 conducts. Resistances R146 and R154 imposes the VGS of P channel MOSFET Q12 to be negative, which turns the MOSFET Q12 on and the obtained +15V_LV follows the voltage LV_BAT. During this period, the Zener diode D14 is blocked and thus Q10 is off, same as Q11.

b. When LV_BAT is larger than 15V, the VQ10b attains the threshold of Zener diode D14: Vbe+VD14, Q10 is thus active, same as Q11. Under this circumstance, the Vgs of P channel MOSFET Q12 increase (due to voltage divider by R146 and R152), which forces the MOSFET to transit from linear region to saturation region, and the voltage difference between LV_BAT and +15V_LV is supported by the drain-source voltage of MOSFET Q2. Through this regulation, the LV supply voltage is limited to +15V.

When abnormal voltage appearing at the battery side (higher than 18V), converter should be stopped immediately. An over voltage protection circuit is designed to turn off the LLC converter if over output voltage appears, as shown in the following figure.

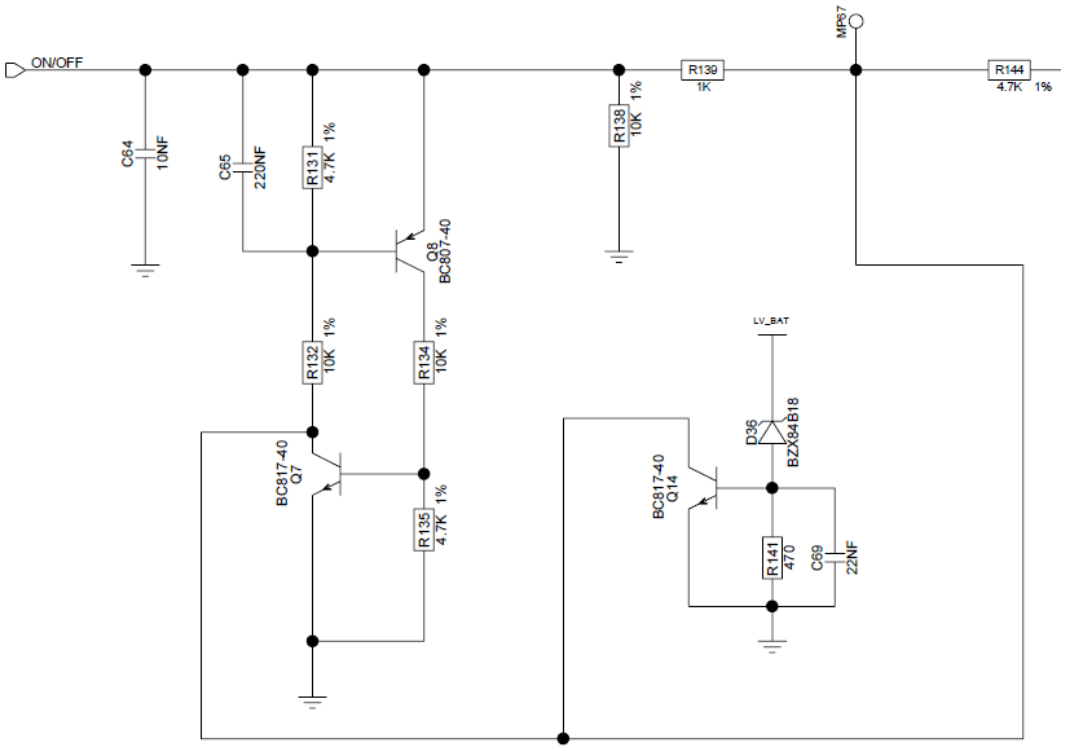


Figure 3-22. Over voltage protection circuit designed for the LLC converter

When LV_BAT attains higher than the threshold voltage of Zener diode D36 (18V), D36 conducts and Q14 is saturated, which in turn saturates the PNP transistor Q8 and Q7, the collector of Q7 is driven to 0V and then the voltage at MP67 maintains at 0V. The converter is stopped completely and can't be self restarted. During normal operation, the collector of Q7 and Q14 performs high resistances and has no influence to the ON/OFF command.

The simulation results of the proposed over voltage protection circuit is shown as follows:

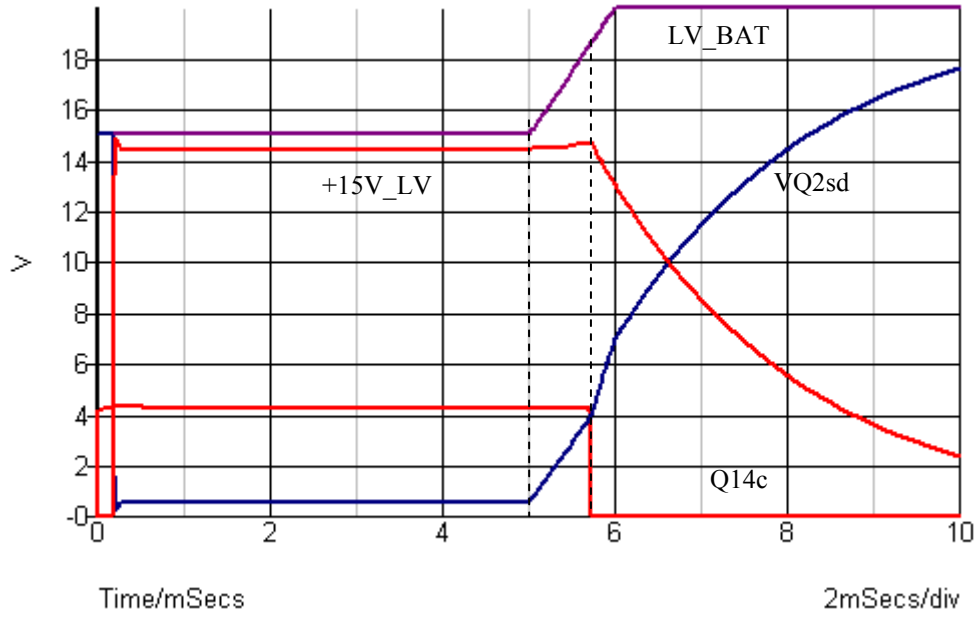


Figure 3-23. Simulation results for LV supply voltage limiting and over voltage protection

In the simulation, a resistor of 50Ω is connected at the +15V_LV to act as a 4W load. As reported by Figure 3-23, the LV_BAT voltage is initially at 15V. LV_BAT rises linearly from 15V to 20V between 5ms~6ms and then remains stable at 20V. When LV_BAT=15V, the supply voltage +15V_LV follows the battery voltage. A voltage difference is detected due to the on resistance of Q2, which causes a voltage drop through the source-drain of MOSFET. When battery voltage rises higher than 15V, Q2 transits to the saturation operation region and +15V_LV is limited to 15V. During this period, VQ2sd increases with the increase of LV_BAT and supports the voltage difference of LV_BAT and +15V_LV. When battery voltage is higher than 18V, the collector voltage at Q14 is reduced to 0 and the converter is turned off.

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Chapter 4. Efficiency Improvement and System Optimization of LLC Converter

4.1 Power module development for LV MOSFETs integration

One challenge of this project is how to handle significant power loss caused by high output current circulating at LV MOSFETs. Standard discrete MOSFETs components are difficult to use here due to limited thermal conductivity and packaging interconnection resistance. More discrete MOSFETs should be paralleled in order to overcome this problem and this increases the overall number of semiconductor devices and increases the overall volume. In this case, an interesting solution is to use a dedicated power module integrating all the LV MOSFETs. [4-1]

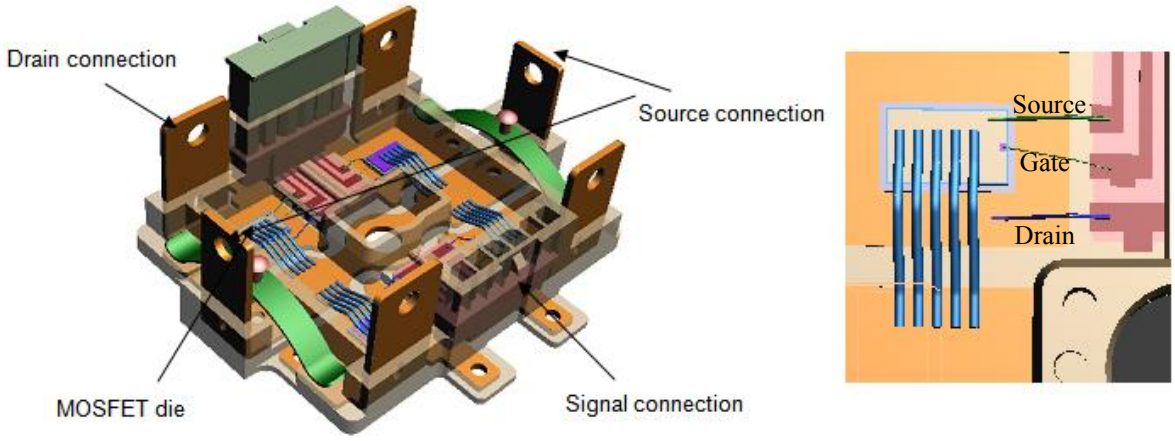


Figure 4-1. Integration of four LV MOSFETs dies in IML power module (3D model).

In this project, an inserted molded lead-frame (IML) power module is designed, shown as in Figure 4-1. Metal lead-frames (0.8mm thickness to offer low conduction resistance) are inserted into a plastic molding, which present horizontal open areas, where the MOSFETs dies are placed and brazed on. Not only holding the bare dies, the lead-frame also spreads to the outside, forming out electrical connection terminals. The designed power module consists of four dies arranged in a double phase configuration, as shown in Figure 4-2. For each MOSFET die, the die's drain is soldered to the metal lead-frame and the process is conducted in a well controlled multi-chamber vacuum oven. This process is important since the solder joint is the first thermal contact layer to the die and needs to be as thermally conductive as possible [4-2]. Solder joint must be checked by an X-ray imaging system to avoid joint voiding. The die's source is connected to the lead-frame by a set of double stitch bondings

(5x500µm or 7x375µm). All the four dies share the same source connections. In order to perform synchronous rectification, small signal connections are drawn out by bondings 125µm. The power module itself is fixed to the cooling plate by screws and turnbuckles.

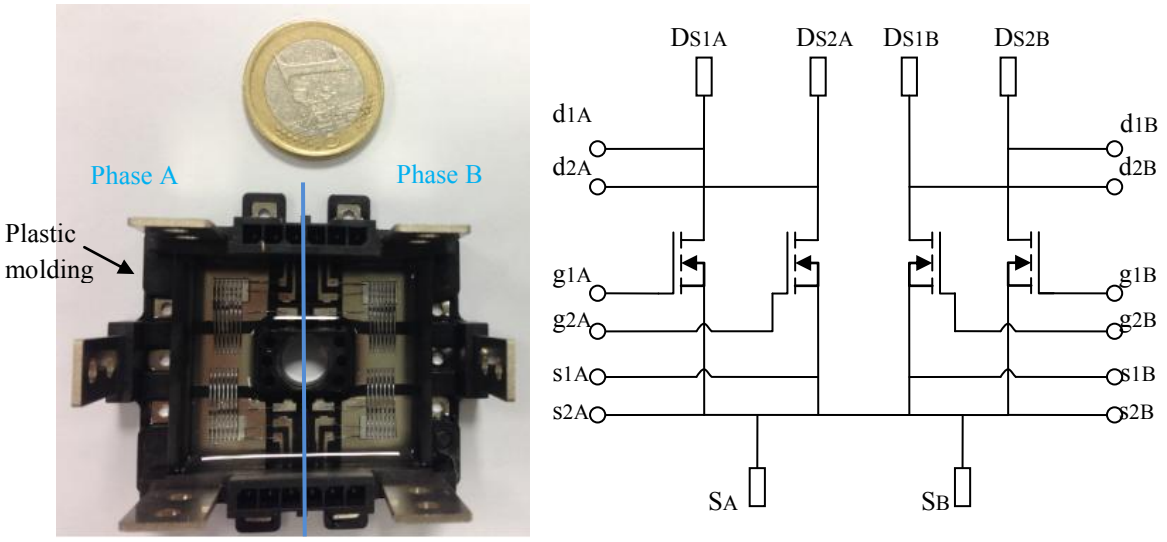


Figure 4-2. Populated IML power module and its equivalent electrical circuits of the designed power module

The lead-frame is made up from copper for high electrical and thermal conductivity. The surface of frame is plated with a thin film of Nickel. At the real power module, 7x375µm bondings are soldered. After bonding soldering, the modules undergo a cleaning process and finally the module is potted with silicone gel which protects the electronics components from dust and moisture. The adopted bare die is Infenion IIPC22S4N06, with an internal resistance Rdson=1.3mΩ, a gate charge of Qg=208nC and a breakdown voltage of VDSS=60V. The total resistance including metal lead-frame is less than 2mΩ.

The main advantage of adopting IML power module is that the heat dissipation of MOSFETs dies is greatly facilitated through the metal lead-frame. But we should take care that the IML module's bottom side is exposed and can cause short circuit if not properly insulated. A thermal interface (BFG30A, c=5W/mK, 300µm) should be inserted below the power module to ensure an electrical insulation between lead-frame and cooling-plate. The thermal characteristics of designed module are shown as in Figure 4-3.

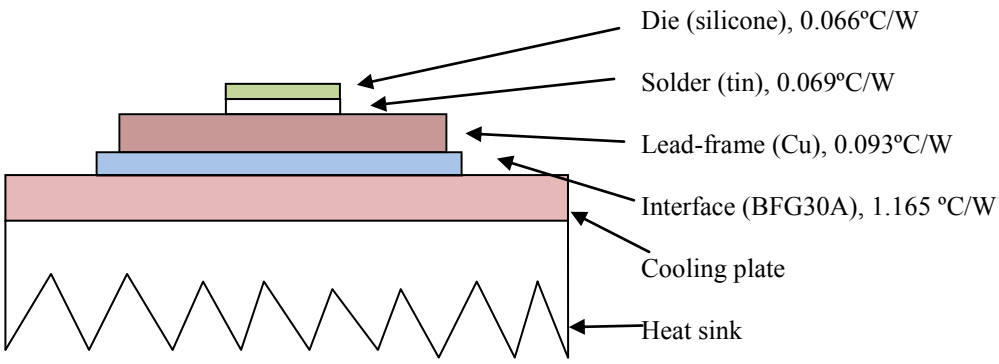


Figure 4-3. Thermal resistances of IML power module.

The total thermal resistance from the MOSFET die to the cooling plate is: Rth=1.393 ºC/W. Supposing a power loss of 15W of each MOSFET (referring to the part 4.3), a temperature difference of about 20ºC is expected between the cooling plate and the MOSFET dies. It can be concluded that IML power modules have significant advantages in thermal performances over discrete FET components. Fewer components, simpler assembly and good current carrying capability can be obtained with the proposed IML power module technology.

4.2 Transformer Design and Improvement

4.2.1 Core Material Analysis and Selection

LLC converter generally requires a very low magnetizing inductance to allow high output power and large scale Vout/Vin regulation capability. In the targeted convertor prototype, the calculated magnetizing inductance is Lm=42uH for input voltage variation range [330V 410V] (Lm=24μH for variation range [220V 410V]). With 16 turns at the transformer's primary side, magnetic cores with a low inductance factor A_L≈165nH should be selected. Two types of materials are available for constructing a core with such a low inductance factor: low-permeability magnetic material or gapped soft-ferrite material.

Low permeability magnetic core realizes a low relative permeability by distributed air-gap. For example, MPP cores (magnetic molypermalloy powder) are cores with distributed air gap made from 81% nickel, 17% iron and 2% molybdenumalloy powder. Kool Mμ core also realizes a low permeability by distributed air gap made from a ferrous alloy powder. They exhibit soft saturation with higher saturation induction level. Table 4-1 shows a comparison result of magnetic characteristics for different magnetic materials.

Table 4-1. A comparison of available magnetic materials for core construction

Desciption	Low permeability		Soft-ferrite				
Material	MPP	Kool Mμ	3C94	3C95	3C96	3C97	3F3
μr	14-550	26-125	2300	3000	2000	3000	2000
Bsat	0.65T	0.95T	0.38T	0.41T	0.44T	0.41T	0.37T
Air-gap	distributed	distributed	centralized	centralized	centralized	centralized	centralized
μe tolerance	±8%	±8%	±10%	±1 0%	±1 0%	±1 0%	±1 0%

As low-permeability materials adopts distributed air-gaps to reduce its relative permeability, thus no centralized air-gap is created and thus there is no eddy current loss at the transformer's winding. However, one problem of low permeability material is its high core loss density. At a given flux density Bpk, the core loss density of low permeability core is about ten times more than that of the soft-ferrite. Due to this shortcoming, the low permeability cores are more suitable for designing EMI chokes where the AC flux density is rather limited. Its utilization in transformer or resonant inductor is therefore not recommended [4-3].

The core loss density Pv approximation of a soft-ferrite material can be obtained from an empirical equation (3-1) forwarded by the supplier: [4-4, 4-5]

$$P_V = C_m f^x {B_{pk}}^y (ct_0 - ct_1.T + ct_2.T^2) \text{ (3-1)}$$

In this formula, *f* is the frequency (Hz); Bpk is the peak flux density, which equals to a half of the AC flux swing (T); T is the temperature (℃); Cm, x, y, ct_0, ct_1 and ct_2 are parameters found by curve fitting of the measured power loss data. For most soft ferrite materials, *y* is generally between [2, 3]; *x* is generally between [1, 2]. Peak flux density has a higher weight than operating frequency in transformer's core loss calculations.

According to the Farady's law, the peak flux density of a transformer seeing a square wave voltage can be calculated as follows:

$$B_{pk} = \frac{TV_o}{4N_2S} \quad (3-2)$$

Vo is the output voltage, T is the switching period, S is the core's effective section, N_2 is the number of transformer secondary turns. It is obvious that the transformer's core loss (or peak induction) in LLC resonant converter depends mainly on its switching period *T* and the core's

effective section *S*. To select a proper magnetic material, it is meaningful to compare the relationship of its core loss density (Pv) and peak induction (Bpk) among the switching frequency range, shown as in Figure 4-4 for operating at 150kHz and Figure 4-5 for operating at 250kHz, separately.

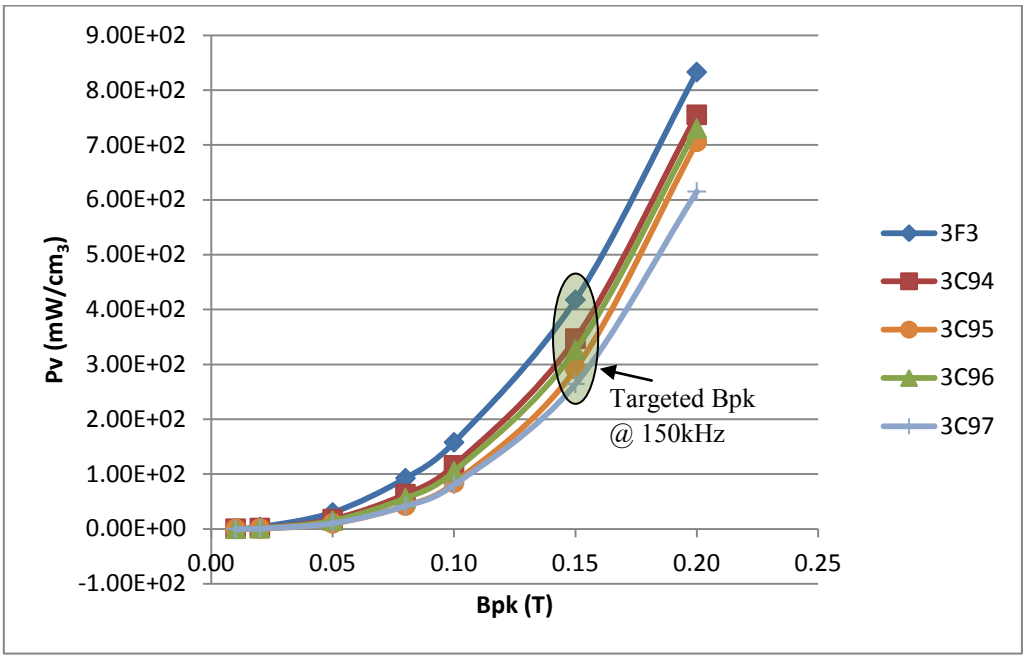


Figure 4-4. Core loss of different magnetic materials at 100ºC, 150 kHz with peak flux density as a parameter

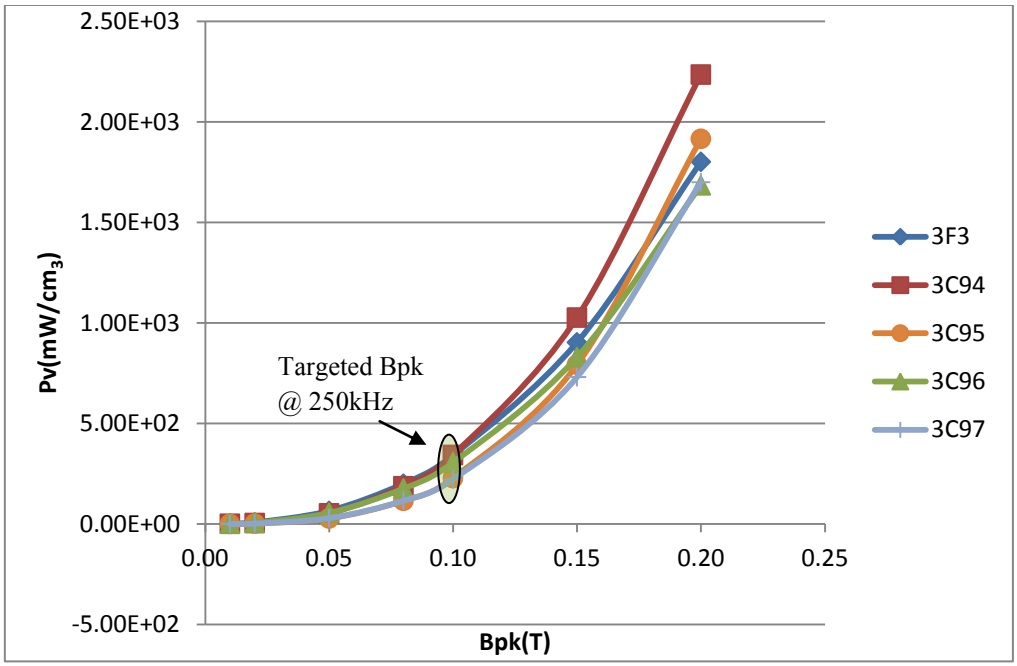


Figure 4-5. Core loss of different magnetic materials at 100ºC, 250kHz with peak flux density as a parameter

The maximum targeted Bpk=150mT is selected to get a good compromise on transformer's volume and core loss. From Figure 4-4 and Figure 4-5, at 150 kHz, the core loss of soft ferrite materials is: 3C97<3C95<3C96<3C94<3F3 at the targeted operating Bpk. At 250 kHz, the core loss density is 3C97≈3C95<3C96<3C94≈3F3. Obviously, 3C97 performs the best core loss density characteristics among the available magnetic materials over a wide frequency range. For the designed LLC converter, the maximum peak flux density appears at minimum input voltage, where the switching frequency is the minimum, which corresponds to Bpk=150mT, *f*=150kHz. Figure 4-6 shows core loss of different materials at 150kHz, 150mT with temperature as a parameter, which corresponds to the operating point with the most core loss.

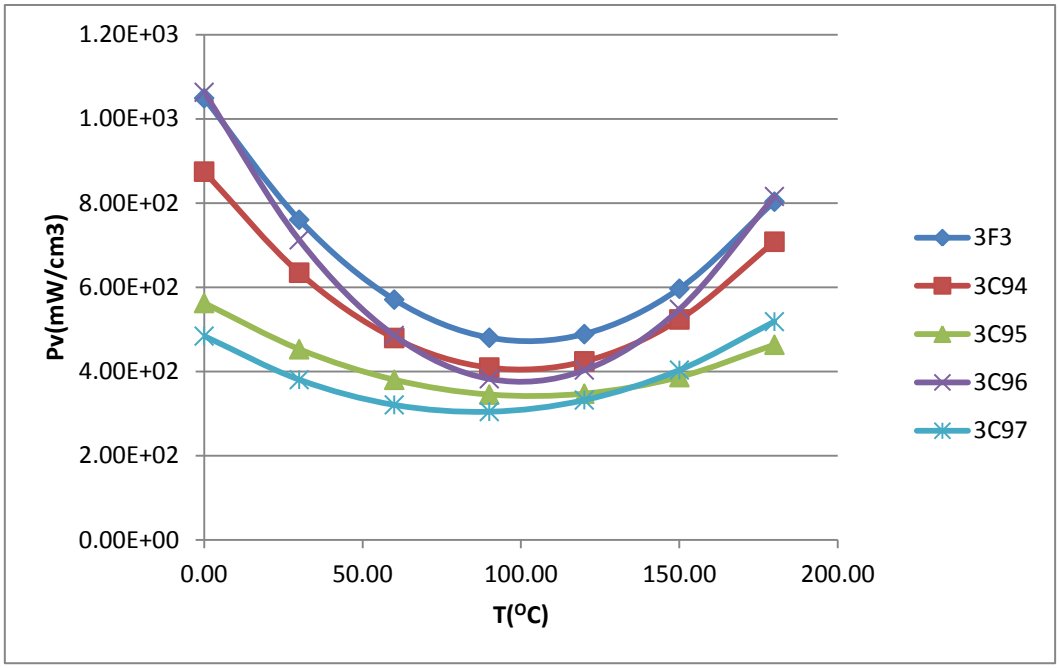


Figure 4-6. Core loss of different magnetic materials at 150kHz, Bpk=160mT with temperature as a parameter

As reported in Figure 4-6, 3C94, 3C96, 3F3 materials perform a low core loss at 100°C, but increasing or decreasing the operational temperature increase sharply the power loss. Considering that the components' operating temperature is under 120°C (referring to the part 4.4 for air-cooling system design), 3C97 have a better performance than 3C95 material,

whereas 3C95 is preferred for operating at a temperature higher than 120^{o}C. 3C97 material is finally selected as the proper magnetic materials for transformers and resonant inductors.

4.2.2 Transformer design and resonant inductance integration

Thanks to the benefits brought by resonant topology, LLC converter is capable to operate at a frequency much higher than PWM converter (150-250kHz in this project). In most of PWM converters and series resonant converters, planar magnetic cores and multilayer PCB are frequently employed in order to get a smaller height, larger dissipation area and more facilitated assembly. In these structures, the transformer's magnetizing inductance value is very high so that no air-gap is needed [4-6]. However, LLC converter's magnetizing inductance should be maintained at a low value to achieve a large ZVS region thus a large air-gap is always unavoidable to attain the desired inductance value. Planar structure has difficulty in integrating a large air-gap due to its limited height and large section. Fringing flux penetrates the PCB winding hence very high eddy current is generated and it results in a high winding loss. Furthermore, the PCB layer's thickness should be kept at a very low value to avoid the skin-effect and the proximity effect caused by a higher switching frequency thus reduces its dc resistance. As a result, it is difficult to continue to adopt the planar structure with multilayer PCB board for the transformer with low magnetizing inductance. Traditional E cores, EI cores or U cores which can integrate a large air-gap are more suitable to attain the required magnetizing inductance. As to the windings, the Litz wire, which is less sensitive to the internal and external flux are generally adopted to get better performances. The primary winding is wound by 16 turns of Litz wire 800 strands of 44AWG (0.05mm diameter each strand, insulated by Kapton 2.5kV), the two secondary windings are wound by the 1200 strands of 44AWG with 4 turns in parallel. To create the required Lm is not a problem; an adequate air-gap length should be selected to get the desired inductance value. In this case, the adopted core is Ferroxcube E42/21/15-3C97 and the created air-gap length is selected to 1.96mm (to realize Lm=24μH, the air-gap length is 3.96mm, this will be discussed later for comparison).

It is possible to study the value of the leakage inductance by modeling the transformer core and windings in a finite element simulation software. Imposing the total ampere turns to zero ($N_1I_1+N_2I_2=0$), the effect of magnetizing inductance is thus annulled and the residual magnetic field energy reflects the total leakage energy [4-7]. The reflected total leakage l_{ft} inductance can then be calculated as follows:

$$\frac{1}{2} l_{ft} I_{rpk}^2 = E_p \quad (4\text{-}2)$$

E_p is the residual magnetic field energy at the full space, which can be obtained through FEMM simulation. I_{rpk} is the peak value of imposed sinusoidal current at the primary side (equals to the resonant current). Following the equation (4-2) and FEMM simulation, it is possible to obtain a simulation result of leakage flux distribution and leakage inductance but it is difficult to know how this leakage inductance is distributed between primary or secondary side. As it is interesting for LLC converter to integrate more primary leakage inductance, one solution to determine the primary inductance is by direct measurement.

Various transformer realization methods are proposed and compared here. One conventional winding method, as shown in Figure 4-7, is to wind the 16 turns of primary at the inner layer across the coil former and the secondary at the outer layer. An insulation material is always needed to be inserted between the primary and secondary to keep a high insulation voltage. Each secondary winding is made up of 4 turns in parallel. Simulation results show the leakage flux distribution and the induction magnitude along the cross-section of the transformer (red line).

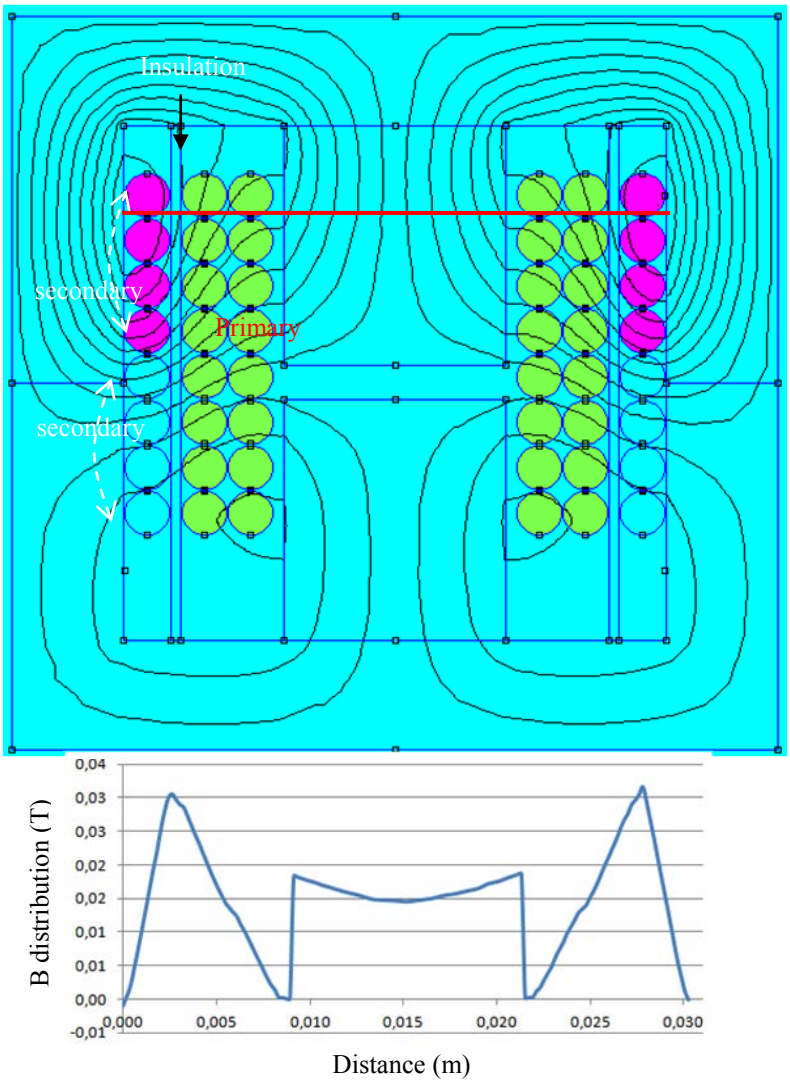


Figure 4-7. Leakage induction distribution for transformer structure I, *lf*=320nH

In this transformer structure I, the primary windings is covered by the secondary winding. During operation, leakage flux traverses the window area, induction increases and decreases linearly at the window area along the transverse axis. The induction is the highest at the inter-space between primary and secondary windings, with a Bpk≈30mT. No induction is detected at the center leg and air-gap. This conventional transformer winding method obtains a good coupling effect with low leakage inductance. In this case, nearly the totality of resonant inductance should be made by an additional resonant inductor.

Higher leakage inductance is possible to be realized by separating the secondary windings from the primary windings. Structure II shows another possible winding solution by winding the 16 turns of primary winding at the center and secondary winding at two extremities, shown as in Figure 4-8.

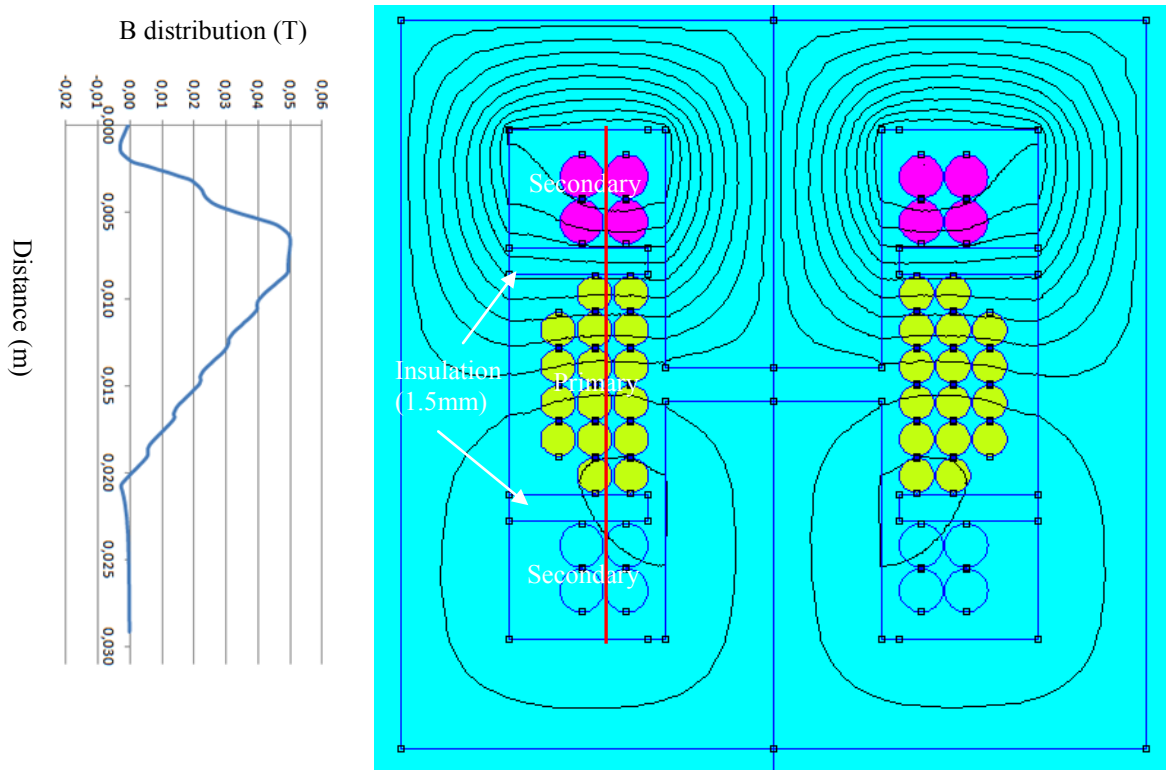


Figure 4-8. Leakage induction distribution for transformer structure II, l_f=1.5 µH

It is more interesting to study the flux density magnitude along the vertical axis of window area (see the red line). As shown in Figure 4-8, higher flux density is detected at the insulation layer, Bpk≈50mT. With a large inter-space between primary and secondary side, this transformer performs a higher leakage inductance of l_f= 1.5µH. The remaining resonant inductor shall be completed by an additional RM12 core, with 6 turns. A photo of transformer prototype is shown in the Figure 4-9.

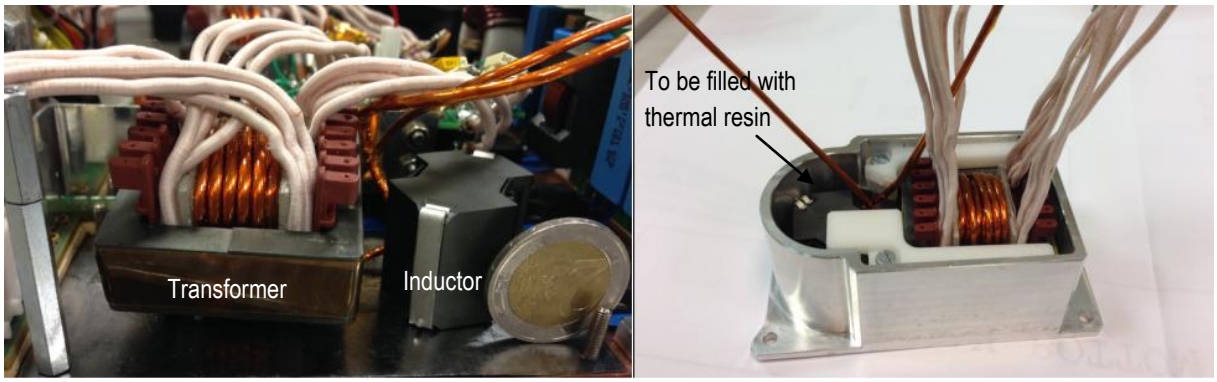


Figure 4-9. Transformer structure II, with additional resonant inductor RM12 without cooling container (left) and in a cooling container (right)

In order to integrate more leakage inductance and get a satisfactory compromise on system's volume, performance and mass, a new concept of inserting a magnetic shunt between the primary and secondary windings is proposed to get an easy-to-regulate leakage inductance integrated into the transformer. The author of paper [4-8] describes this idea and applies it in an X-compressed planar transformer for series resonant inductor. The author of [4-9] introduces the Ferrite Polymer Composite (FPC) material [4-10] to the construction of a 1kW E structure LLC resonant converter and obtains satisfactory results. FPC film is a thin, mechanically flexible film with a low permeability μr=9 (for material C350 and C351) or μr=17 (for material C302). From the datasheet forwarded by the supplier, it is available in 0.2mm and 0.3mm thicknesses, and performs an insulation voltage of 1kV/mm. As shown in Figure 4-10, the insulation layer is replaced by the FPC film with a relative permeability μ_r=9, 1.5mm thickness to create a magnetic shunt between primary and secondary windings.

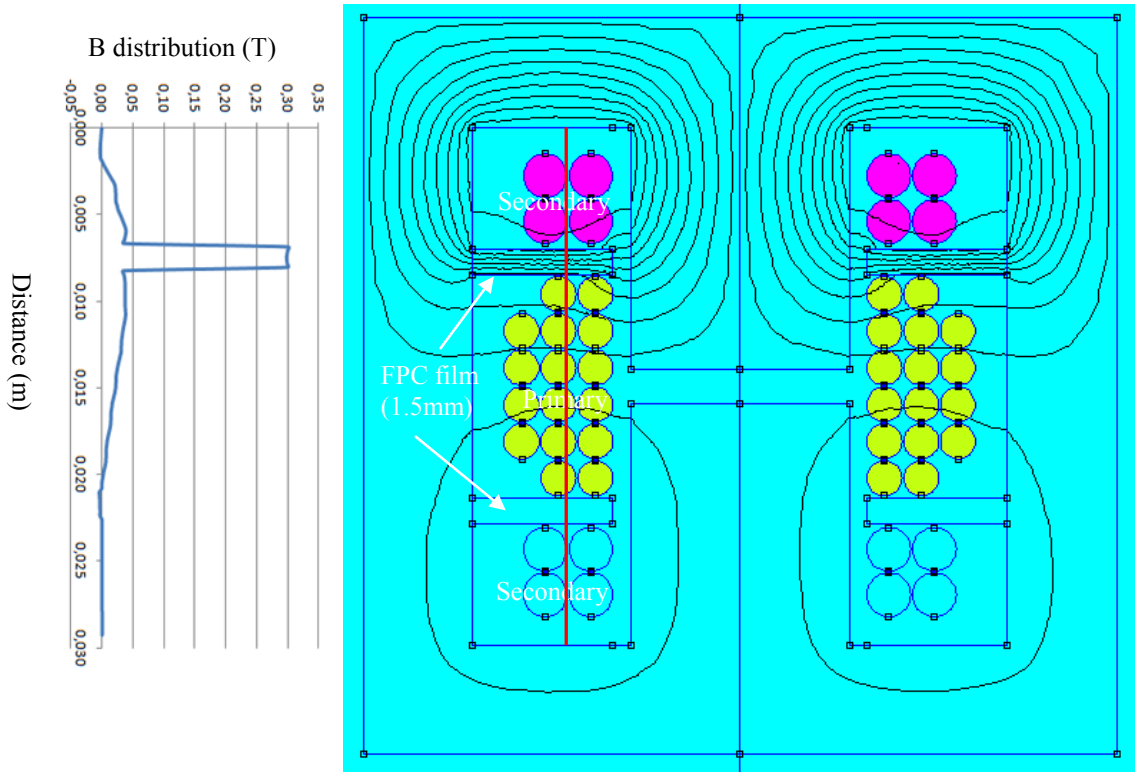


Figure 4-10. Leakage induction distribution with FPC film insertion, structure III, *lf*=3.8uH

As shown in Figure 4-10, leakage flux is concentrated at the FPC film due to a low reluctance created, with Bpk≈300mT. Higher magnetic field energy is stocked at the inserted FPC film. Simulation results show that a leakage inductance of 3.8μH is created. As the targeted

resonant inductance is 7.5μH, this transformer structure has already integrated 50% resonant inductance while the additional part needed to be compensated by a resonant inductor is half reduced. The following figure shows a photo of the transformer with FPC film material insertion.

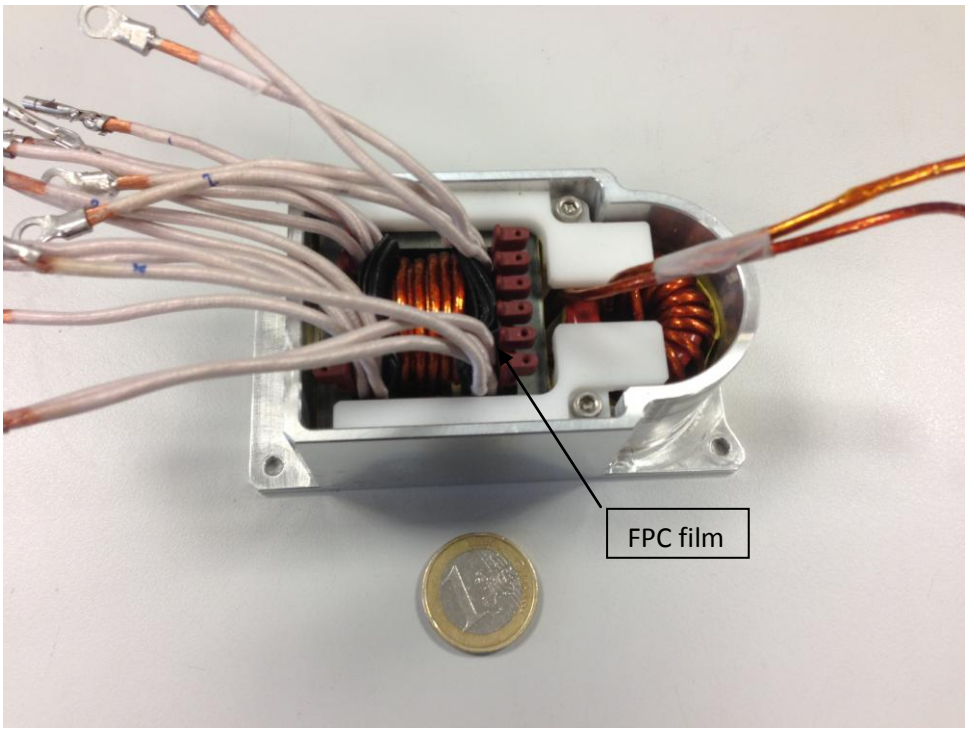


Figure 4-11. Transformer structure III, with FPC material separating primary and secondary windings

Despite advantages brought by FPC material in integrating higher leakage inductance, some limitations exist when applying this method into practical applications. Firstly, as leakage flux passes through the magnetic shunt, a relatively high flux density is generated which causes an extra power loss. FPC film has higher core losses than soft ferrite magnetic materials. Considering that this film is stacked with the windings and is difficult to be cooled, an internal regional high temperature may appear. Secondly, leakage inductance value tolerance is another important issue that should be taken into consideration. In the structure II, the leakage flux is fixed by the core's structure and bobbin's geometry and all the leakage flux passes through air whose relative permeability is constant μr=1, making it not sensitive to atmosphere and operational condition changes. As to the transformer structure III, flux linkage passes through the FPC film whose relative permeability is subjected to a tolerance of ±20%. ±20% resonant inductance variation causes a maximum ±9% variation of the resonant frequency. These two drawbacks reduce its interest in transformer design.

Another possible approach to integrate more leakage inductance is to use the U core and separate the primary and secondary windings at different core legs. Under the same branch leg width, the U core's depth should be doubled to get the same effective section, but the air-gap can be distributed to two legs thus the gap length at each leg is half reduced. Winding primary side at one leg and secondary side at the other leg results in a poor coupling thus a high leakage inductance can be retained. The following figure shows the simulation results of proposed transformer based on a U30/21/30 core (not a standard core, 30/21/30 means half core's width, length and depth in mm, respectively).

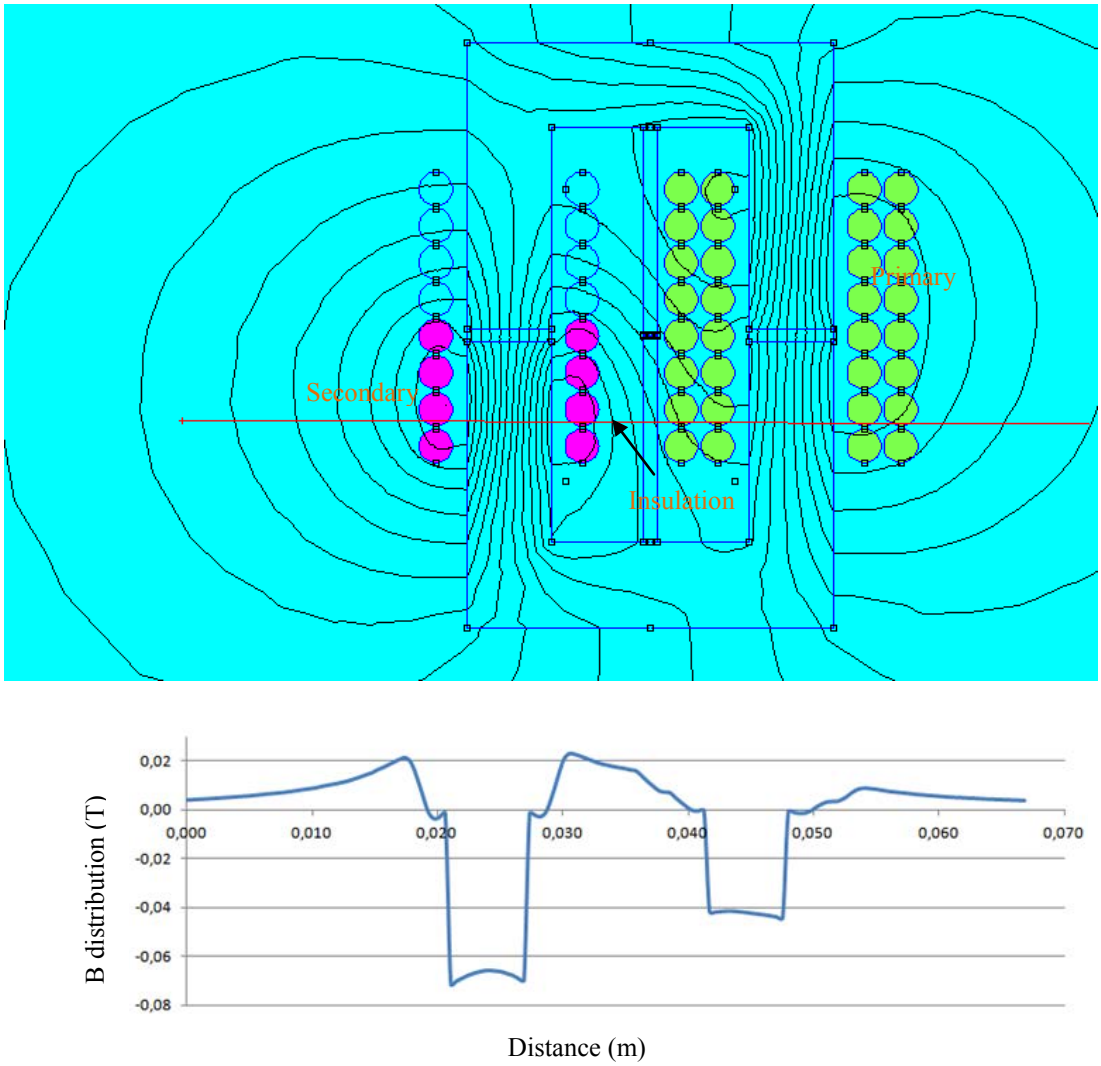


Figure 4-12. Leakage induction distribution of transformer structure IV, *lf*=7.5uH

U core transformer creates a high leakage inductance naturally and can integrate the totality of resonant inductance. The leakage inductance can be regulated by adjusting the core's window width: separating the primary winding from the secondary winding increase the magnetic field energy stored at the window area thus increase its leakage inductance, vice versa. But

unlike the E cores whose magnetic field energy is limited at the window area, the magnetic field energy of U cores is dispersed to the outer space. At the prototype, the aluminium cooling plate and the control circuit PCB board are thus exposed to the leakage flux, causing extra eddy current loss at the cooling plate and making the circuit operation threaten by radiated electro-magnetic induction. A transformer prototype of structure IV has been designed and constructed (Figure 4-13); we found by experimentation that the synchronous rectification circuit is disturbed by the leakage flux. Moreover, the power loss of the whole prototype is not improved. The extra eddy current loss caused by leakage flux is more costly than that of a resonant inductor. Furthermore, in order to attain the targeted *lf* value, the core's mechanical dimension should be carefully studied and designed, which frequently results in a non industrialized magnetic components and adds the cost. Thus the U core structure is not a good candidate for LLC transformer solution.

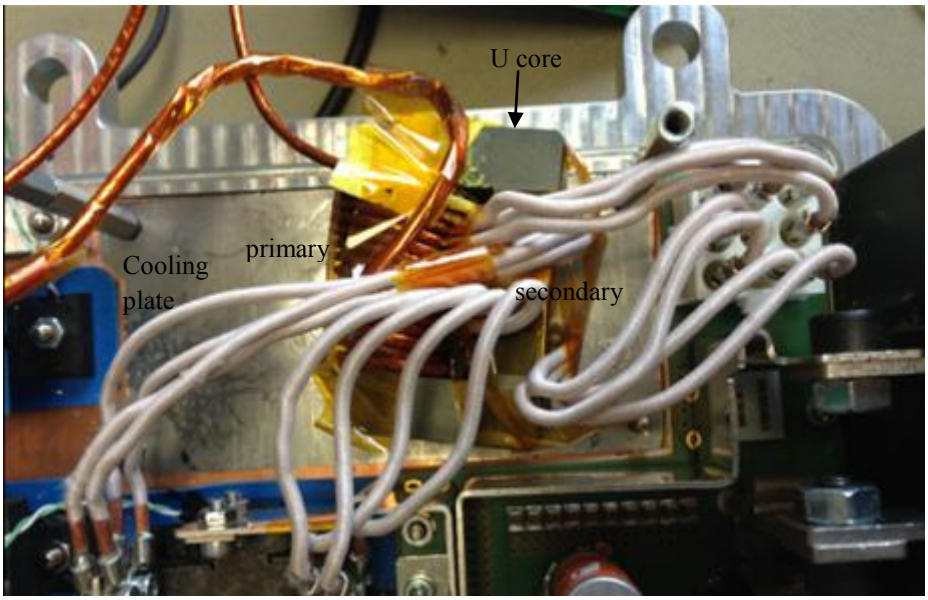


Figure 4-13. Transformer structure IV mounted at the proto, with U cores integrating the resonant inductor

In conclusion, the transformer structure II is finally selected. Its advantages are mainly: leakage inductance partially integrated into transformer, leakage inductance with limited value dispersion, commercialized magnetic components, low EMC radiation, etc. The transformer design details are summarized in the following table.

Table 4-2. Transformer design summary by structure II

Description	Types	Values
Transformer Magnetic core	Core type	E42/21/15-3C97
	Inductance factor (AL)	170nH
	Effective area(Ae)	1.78cm^2
	Volume(V)	17.3cm^3
	Air-gap length(e)	2mm
	Magnetic inductance (Lm)	42μH
	Leakage inductance(lf)	1.5μH
	Peak induction (Bpk)	160mT
Transformer Wire	Primary turns (N1)	16
	Primary wire size	Round Litz 800 strands of 44AWG, Kapton insulated
	Secondary turns (N2)	1
	Secondary wire size	Round Litz 1200 strands of 44AWG, 4 in parallel
	Fill factor	80%
	Primary AC resistance (Rac_p)	25mΩ
	Secondary AC resistance(Rac_s, including external connections)	1.5mΩ

For the design of resonant inductor, the design process is simple. Different from transformers, the magnetic core in resonant inductors serves only to guide the magnetic induction. The dimensioning of resonant inductor is to select a proper core with proper air-gap volume to satisfy the requirement for energy storage in resonant inductor.

$$\frac{1}{2} l_{r\_add} I_{rpk}^2 = \frac{1}{2} BHV_{gap} = \frac{B_{pk}^{\ 2}}{2\mu_0} A_e e \quad (4\text{-}3)$$

In equation (4-3), l_{r_add} is the targeted additional resonant inductance; Ae is the effective area of selected magnetic core. Material's core loss property suggests a maximum peak induction. Selecting the maximum B_{pk}=150mT, a minimum air-gap volume can be derived from the above equation (4-3) Vgapmin=0.113cm^3. From the supplier's catalogue, a suitable magnetic core which satisfies the minimum gap volume should be selected. Finally, the selected

magnetic core is RM12/I-3C97, with Vgap=0.196 cm^3 and the final Bpk=114mT. The designed resonant inductor dimensioning is shown in the following figure.

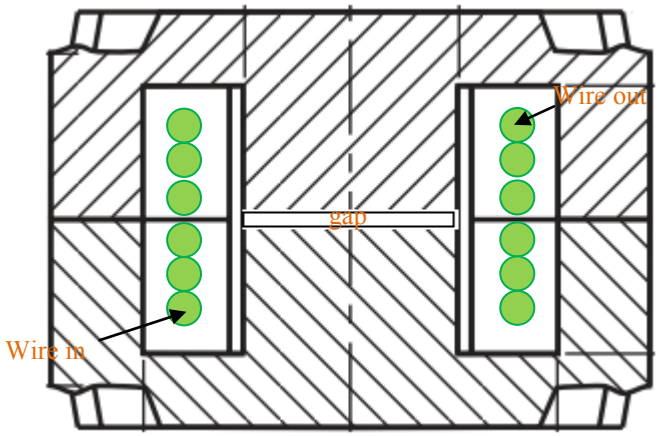


Figure 4-14. Resonant inductor designed in RM12/I core

We use the same wire for realizing the transformer's primary winding and inductor's winding, in order to avoid an external connection between these two components. The inductor design details are shown at the Table 4.3.

Table 4-3. Resonant Inductor design summary

Description	Core type	RM12/I-3C97-A160
Inductor magnetic core	Inductance factor (AL)	160nH
	Effective area(Ae)	1.46cm^2
	Minimum effective area(Aemin)	1.25cm^2
	Volume(V)	8.34cm^3
	Air-gap length (e)	1.57mm
	Resonant inductance (Lr)	6μH
	Peak induction (Bpk)	114mT
Inductor wire	Wire size	Round Litz 800 strands of 44AWG, Kapton insulated
	Number of turns (N)	6
	Fill factor	60%
	AC resistance (Rac, including external connections)	10mΩ

4.2.3 Eddy current loss study

Litz wire is composed of copper conductors made up of multiple individually insulated strands twisted or woven together. It is generally used to avoid skin effect and reduce proximity effect of windings in transformer construction. As insulators are inserted among different strands, Litz wire then has a poor thermal conductivity compared to pure copper wire. If not properly designed, heat produced by Litz wire will be difficult to be dissipated and the wire strands may be melted. Therefore, the power losses of Litz wire should be precisely estimated and controlled. The power losses of Litz wire is shown in the Figure 4-15. [4-11]

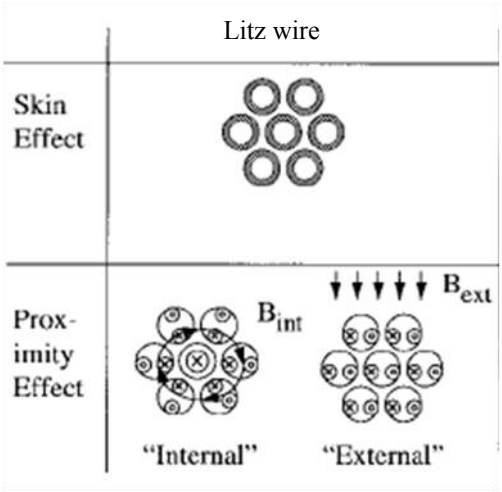


Figure 4-15. Types of power loss in Litz wire

In Litz wire, the diameter of each strand should be less than the skin depth defined in the following equation:

$$\sigma = \sqrt{\frac{2\rho}{\omega\mu}} \quad (4-4)$$

Under this condition the current distribution is expected to be homogenous. However, considerably high loss can still be generated due to proximity effect. It may still further be divided into internal proximity effect and external proximity effect. Internal proximity effect is the current distribution effect affected by the adjacent strands and windings. As shown in Figure 4-15, the surrounding strands are influenced by the induction generated by the central strand. When the number of strands becomes large, all the strands have an influence on its

adjacent stands and the mutual interaction is significant. [4-11] proposed an equation to calculate the ac resistance caused by internal proximity effect in a defined winding area filled with Litz wire strands, based on the further development of Dowell function. The proposed equation is possible to predict the ac resistance of transformer winding composed by Litz wire under no external field. When Litz wire is exposed to an external magnetic field generated by transformer's air gap, fringing flux penetrates into the Litz wire and the equation described in [4-11] is no further applicable.

In order to analyze the eddy current loss when wire is exposed to an external flux Bpk, an equation is proposed to approximate the loss where conductor's diameter is smaller than skin depth [4-12], [4-13], [4-14]:

$$P = \frac{\pi\omega^2 l {B_{pk}}^2 d^4}{128\rho} \quad (4-5)$$

Where ρ is the resistivity of the conductor, d is the diameter of the wire, l is the length of the conductor, B_{pk} is the peak external magnetic field perpendicular to the axis of the wire at a radian frequency ω. One turn of Litz wire with N strands exposed under a certain magnetic field can then be approximated as follows:

$$P_{eddy} = N\frac{\pi\omega^2 l B_{pk}^2 d^4}{128\rho} \quad (4-6)$$

The total primary winding loss of Litz wire then can be expressed by:

$$P = P_r + P_{eddy} = I_{rrms}^2 R_{ac} + N\frac{\pi\omega^2 l B_{pk}^2 d^4}{128\rho} \quad (4-7)$$

Where Rac is the dc resistance of the Litz wire, Rac≈Rdc for d<σ; Irrms is the RMS value of resonant current. In order to further explore the relationship of eddy current loss and each strand's diameter, the equation (4-6) can further be written as:

$$P_{eddy} = \frac{4\omega^2 l B_{pk}^2 d^2 S}{128\rho} \quad (4-8)$$

Where S is the total effective conductive section of Litz wire, $S = N\pi d^2/4$. From equation (4-8), it is obvious that under the same total effective conductive section S, decreasing the strand diameter greatly reduces the eddy current loss in a Litz wire. To obtain a low eddy current loss, choosing a large number of fine strands and decreasing the strand's diameter is

an effective solution. However, as the number of strands increases, the fraction of the window area filled with insulator increases and these results in an increase in dc resistance. Furthermore, finer strands are more expensive and difficult to precisely control its configuration. Thus the strand diameter should be carefully selected and verified for efficiency, feasibility and cost compromise. Paper [4-11] has proposed a recommended strand diameter selection criteria for Litz wire, d=σ/4~ σ/3. In this dissertation, we select Litz wire 800*44AWG with d=50μm (~ σ/3).

In order to estimate the eddy current loss of the proposed transformer, it is possible to obtain calculation results from equation (4-6) based on simulations at FEMM software which gives the Bpk value at each Litz wire's section. Or we can obtain the eddy current loss results directly from FEMM software. For Litz wire model, FEMM cannot plot the current distribution of each strand, but it is possible to compute an eddy current power loss at each wire's cross section.

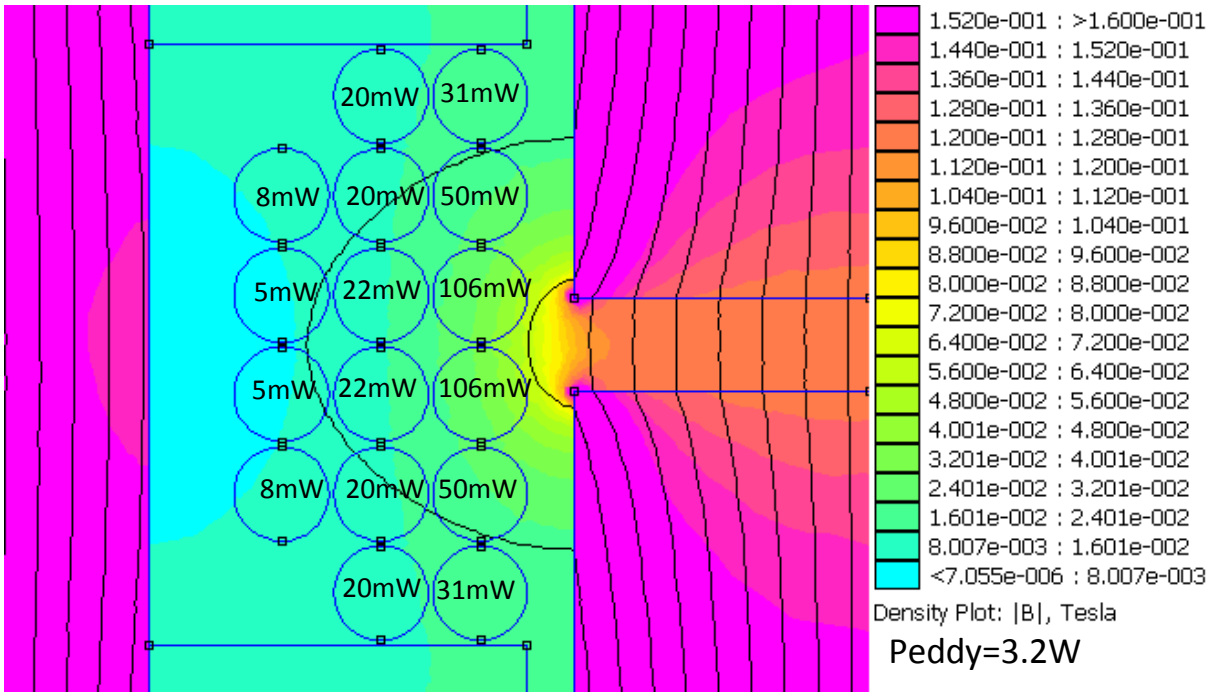


Figure 4-16. The eddy current loss simulation results for primary windings

Simulation reported in Figure 4-16 shows the eddy current loss of each primary conductor at the left window. FEMM is 2D simulation software while the wire length is defined to be the same length to the core's height, that is 15mm. Considering that the average length of turn is 93mm for this magnetic core, the total eddy current loss should be the sum of all the 16 turns

then multiplied by 6 (~93/6). From Figure 4-16, the two Litz wire close to the air gap is penetrated by the fringing flux with Bpk≈60mT, and a large eddy current loss of 106mW is generated for each. For wires far away from the air-gap, fringing flux is gradually reduced and the corresponding eddy current loss is also gradually reduced. Simulation results give a total eddy current loss of 3.2W. By applying simulated peak magnetic field density into the equation (4-6), we obtain a total loss of 3.3W, which is in accordance with the FEMM simulation results.

In order to reduce the eddy current loss, one solution is to create a forbidden zone of 4mmX2mm, as shown in the Figure 4-17.

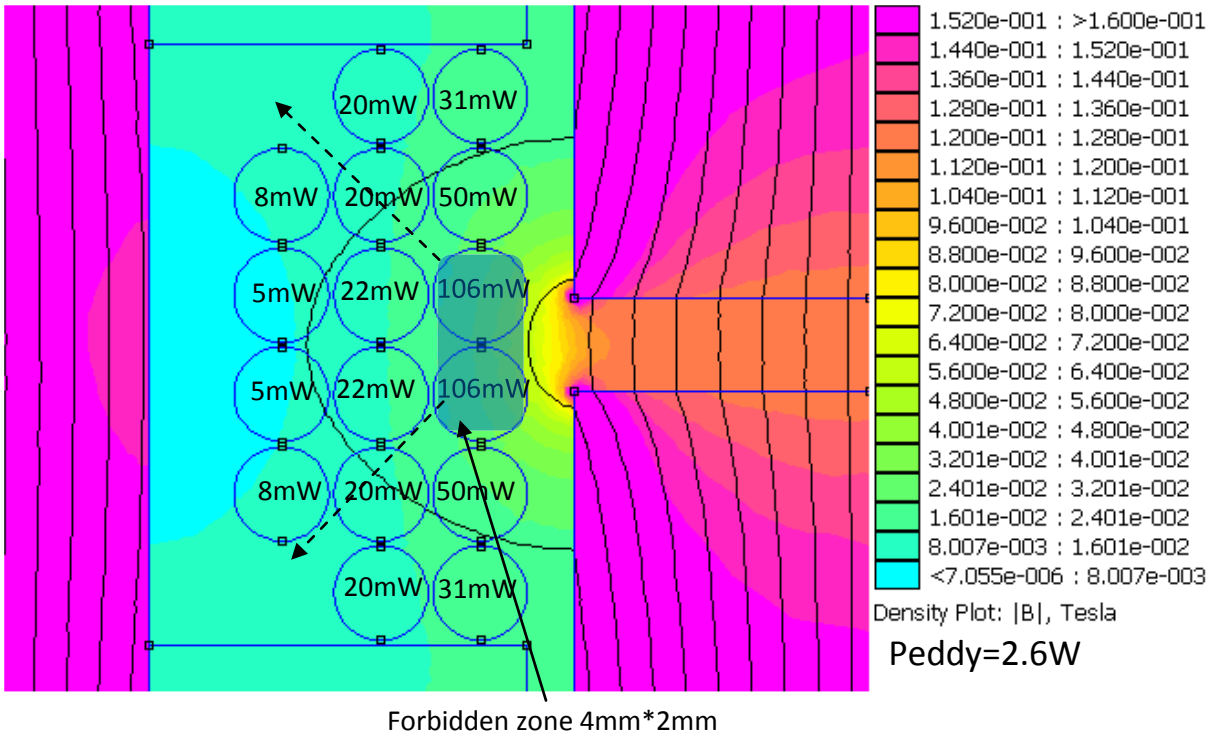


Figure 4-17. Creating a forbidden zone to a get reduced proximity effect

From the Figure 4-17, the two turns closest to air-gap is removed to the outside layer to avoid being penetrated by fringing flux. Eddy current loss is then reduced to 2.6W. Calculation results also give 2.6W. The conception of this winding arrangement is rather simple; however, it is difficult to be realized by transformer suppliers and also difficult for mass production since the forbidden zone is difficult to be created easily. A special form of coil former containing a rectangular forbidden zone needs to be designed. Furthermore, the existence of the forbidden region makes it difficult to automatically wind the Litz wires by a winding machine. All the existed winding machines wind the wires uniformly following a given step

length equal to the wire diameter and it is difficult to skip the forbidden zone automatically. Another proposed method in this thesis relates to insert an insulation layer of about 2mm to keep the windings away from the air-gap, shown as in Figure 4-18:

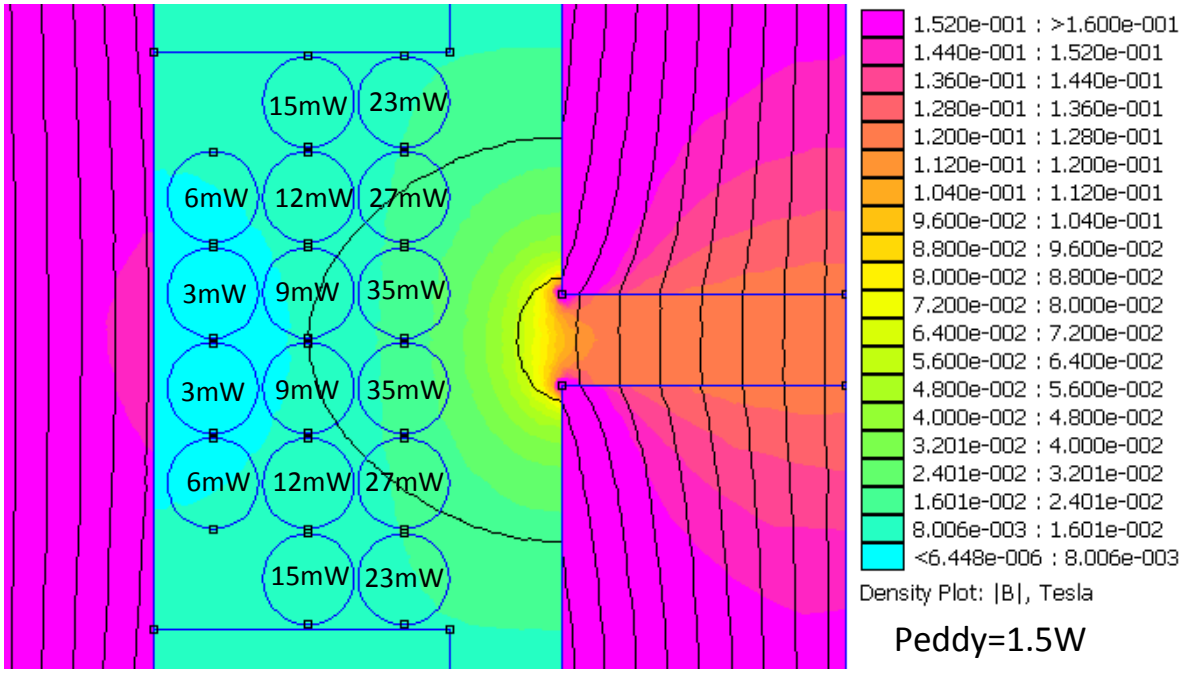


Figure 4-18. Proposal of shifting the primary winding to get a reduced proximity effect

By keeping the windings away from the air-gap, all the primary turns see a reduced magnetic field induction and the proximity effect can further be reduced. The obtained eddy current loss under this case is 1.5W. Keeping the windings away from the air-gap can be realized easily by increasing the thickness of the coil former and this solution is finally adopted in the transformer design at this dissertation.

With the same concept, it is also possible to simulate the eddy current loss when selecting a low magnetizing inductance Lm=24uH for Vin [220V 410V]. In this case, an air-gap of 3.96mm is created and the simulation results are shown in Figure 4-19.

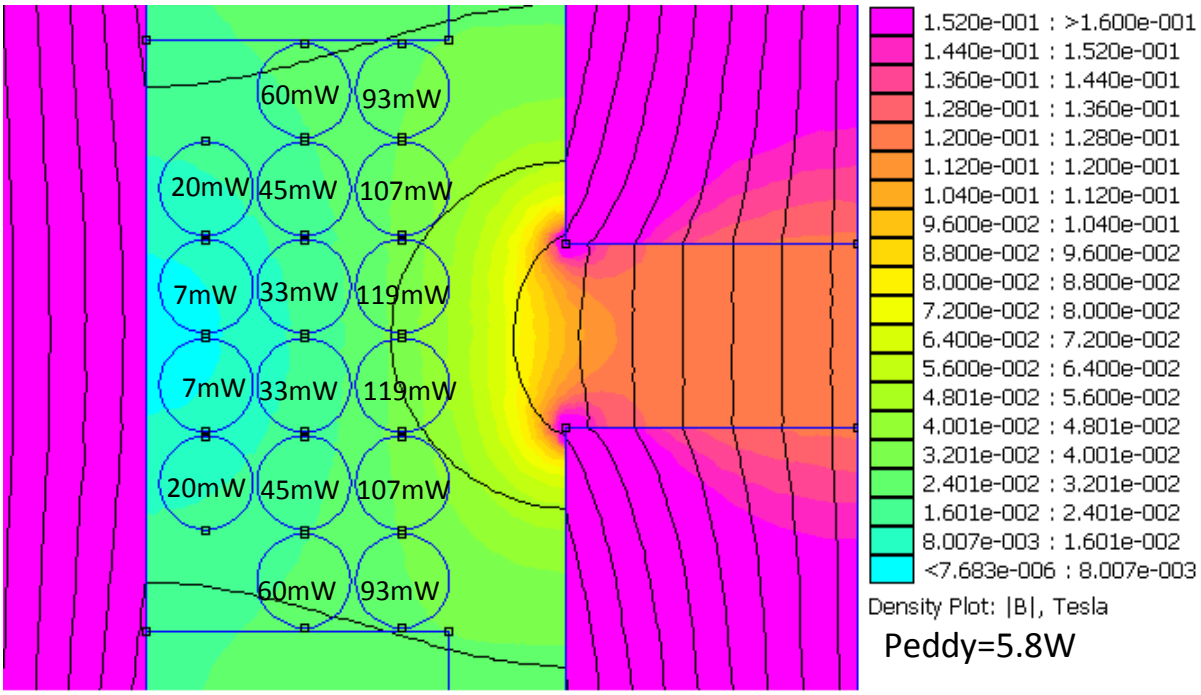


Figure 4-19. Eddy current loss simulation under e=3.96mm for a reduced Lm=24uH

As discussed in the chapter 2, selecting low Lm value permits to get a large input voltage variation range. From the simulation results, it is clear that selecting a low Lm not only increases the reactive current at primary, but also causes a large eddy current loss due to a large air-gap. Detailed experimental results will be presented at the part 4.5.

4.3 Improvement of synchronous rectification

4.3.1 Synchronous rectification and its imperfections in LLC resonant converters

LV side synchronous rectification is necessary to keep a high efficiency since the MOSFETs have a voltage drop equal to $R_{dson}*I_{S1}$ or $R_{dson}*I_{S2}$, rather than a Schottky diode whose forward voltage is at least 0.4V or even higher [4-15, 4-16, 4-17]. The typical waveforms of a synchronous rectification by sensing the drain-to source voltage under LLC resonant converter are shown in the Figure 4-20[4-18].

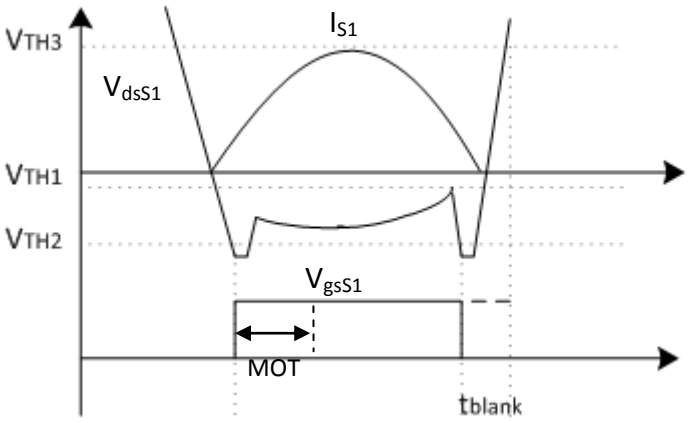


Figure 4-20. Typical waveform of the LV synchronous rectification in a LLC converter by sensing the drain-source voltage of MOSFET

The V_{dsS1} is the drain-source voltage of the MOSFET S_1. V_{TH1}, V_{TH2} and V_{TH3} are the turn-off threshold, turn-on threshold and the reset threshold, respectively. V_{dsS1}, V_{gsS1} and I_{S1} are the drain-source voltage, driving signal and source-drain current of the MOSFET S_1. The operation of a synchronous rectification can be divided into two phase: the turn-on phase and turn-off phase, separately.

A. Turn-on phase

When the conduction phase of the MOSFET is initiated, current will start flowing through its inverse body diode, and a negative voltage will be generated across drain-source of the MOSFET. This voltage drop (normally 0.4-1.5V) is higher than the turn-on threshold V_{TH2} and will trigger the turn on of the MOSFET. As the body diode turns on in prior to the MOSFET, the MOSFET can be switched on in ZVS mode.

The selected SR controller has a function called minimum on time (MOT) that will maintain the MOSFET on for a minimum amount of time. At the end of the each MOT, the controller senses the MOSFET's drain-source voltage. If the V_{dsS1} is higher than the V_{TH1}, the MOSFET is switched-off suddenly and the driver signals for the next period is inhibited. This function is to prevent high reverse conductive current at very light load.

B. Turn-off phase

Once the MOSFET has been switched on, it will remain on until the rectified current decays to a level where V_{dsS1} cross the turn-off threshold V_{TH1} (usually several mill-volts). Once the threshold is crossed, the resonant current is not zero but remains at a very low value and the

remaining current will flow again through the body diode, which causes the MOSFET's drain-source voltage jump negative and could trigger the turn-on threshold. To prevent this case, the V_{TH2} is blanked for some time until V_{TH3} is crossed to avoid the regeneration of the wrong turn-on driving signal and the MOSFET is switched off. During this time period, the drain-source voltage jumps to positive and cross the V_{TH3} which terminates the blank period. The MOSFET is switched off naturally in quasi-ZCS mode.

In the above analysis, MOSFET is considered to be fully resistive and other imperfections or parasite components are not taken into consideration. However, it is difficult to implement the described SR strategy directly to the designed LLC converter. The selected secondary MOSFET die's internal resistance is very low: 2mΩ and thus the Vds across the MOSFET is at several mV levels and is difficult to keep the measurement precision. The measurement is easy to be disturbed by the noises and SR operation error occurs, shown as in Figure 4-21.

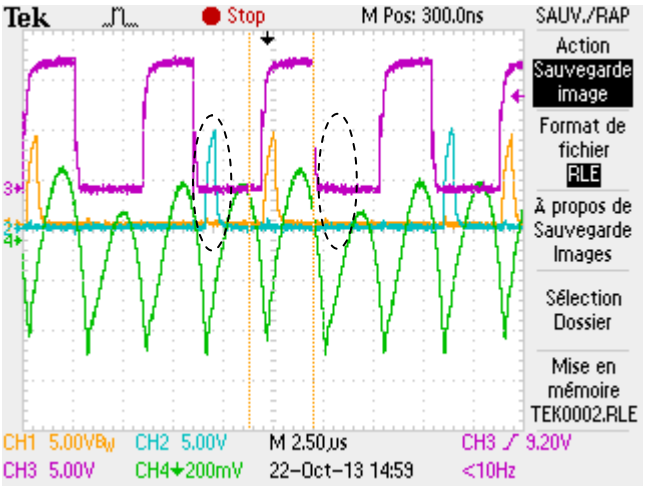


Figure 4-21. Synchronous rectification error at the fault switching-off timing (CH1:VgsS1, CH2: VgsS2, CH3: Vgs_QL, CH4: Is2+Is1)

As shown in Figure 4-21, the SR command signal stops while the current has not fallen to zero but at the end of each MOT. The measurement circuit senses a false voltage higher than $V_{TH1}$and triggers the MOT protection mode, the command stops too early and the command for the next period is also inhibited.

In order to increase the robustness of SR, this paper proposes to include some parasite inductances to the drain-source measurement, shown as in the Figure 4-22.

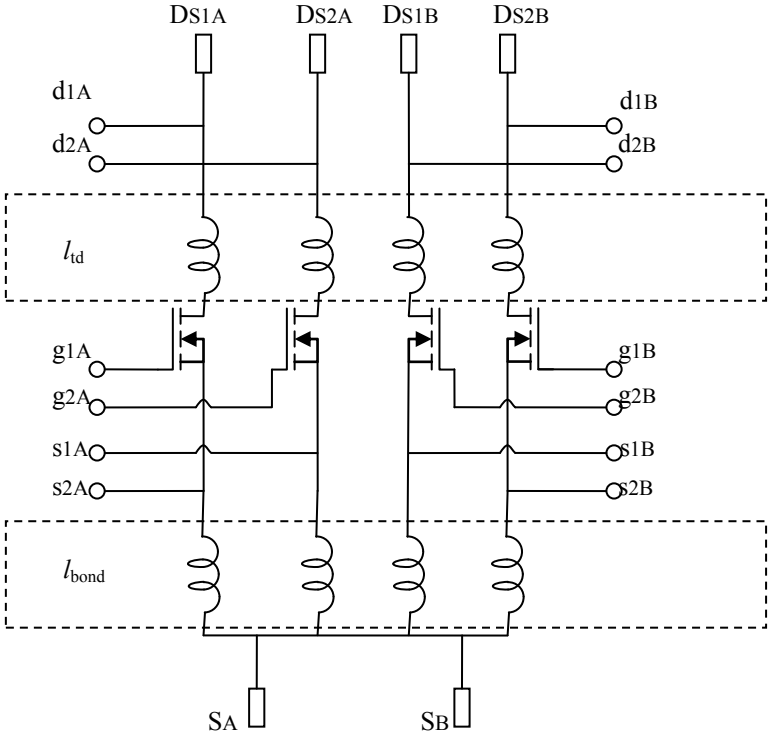


Figure 4-22. Proposed drain-source measurement method to improve the SR robustness

In a MOSFET power module (Referring to Figure 4-1), two types of parasite inductances exist: parasite inductance between drain terminal and die's drain: l_{td} ~10nH, and bonding inductance between die's source and source terminal l_{bond} ~5nH. If we use the power module's drain terminal for the drain signal measurement, this includes the parasite inductance of l_{td} in series with the MOSFET. When current increases, negative voltage is developed at the inductance and this helps to keep a sufficient negative voltage level, to be less sensitive to the noises and avoid wrong MOT protection. Including the bonding parasite inductance is not recommended. When two power cells operate at different frequencies, mutual influence between the two phases results in a SR wrong action by l_{bond}.

Supposing the current flowing through each MOSFET is perfect half-wave sinusoid, the measured drain-source voltage across the MOSFET can be calculated as follows [4-19]:

$$V_{dsm} = -i_s(R_{dson} + j\omega_s l_{td}) = -Is_{pk}\sin[\omega_s t + a\tan(\omega_s l_{td}/R_{dson})]\left|R_{dson} + j\omega_s l_{td}\right| \quad (4\text{-}9)$$

SR duty cycle can be derived as imposing the equation (4-9) to be zero:

$$D_{SR} = \frac{T_{on}}{T_s/2} = 1 - \frac{a\tan(\omega_s l_{td}/R_{dson})}{\pi} \quad (4\text{-}10)$$

From the equation (4-10), due to the presence of the inserted parasite inductance, the duty cycle is less than 1 and the MOSFET is switched-off earlier. The phase lost can be calculated as:

$$P = \frac{a\tan(\omega_s l_{td} / R_{dson})}{2\pi} T_s = \frac{a\tan(\omega_s l_{td} / R_{dson})}{2\pi f_s} \quad (4\text{-}11)$$

It can be seen from the equation (4-11) that the phase lost depends on the operating frequency and the ratio of parasite inductance/ON resistance, not on the output current. The calculated phase lost for f=150kHz to 250kHz is plotted as follows (l_{td}=10nH, R_{dson}=2mΩ):

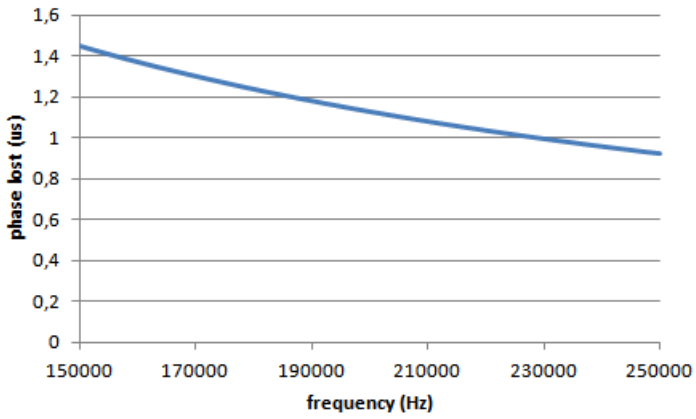


Figure 4-23. Calculated phase lost for applied LV MOSFETs Vds voltage measurement

The following figure reports a simulation result of this effect at nominal power, Vin=330V, *f*=150kHz.

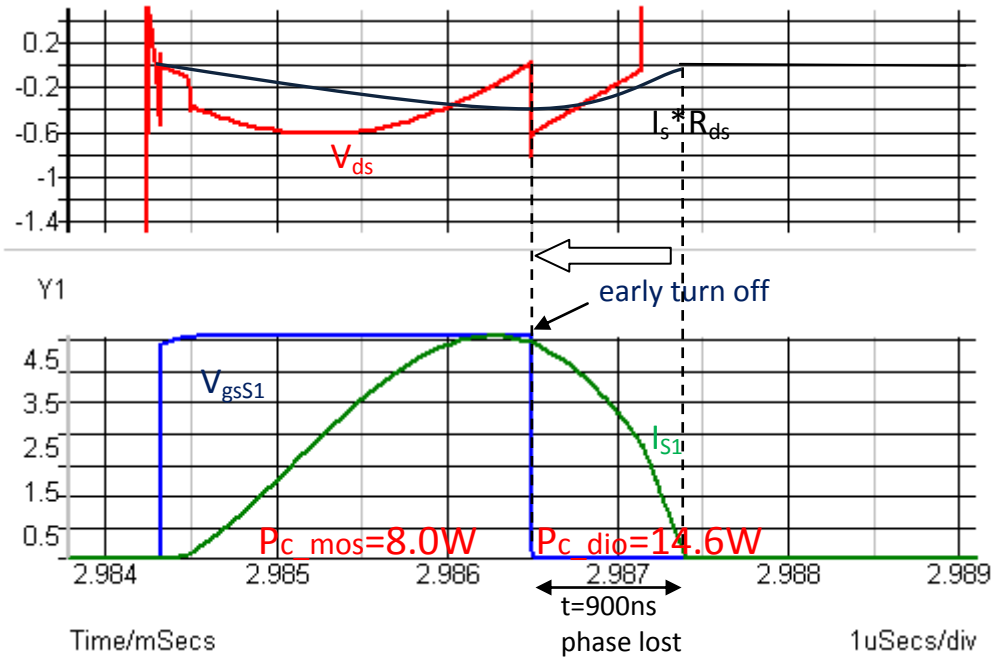


Figure 4-24. SR phase lost results of MOSFETs at nominal power, *f*=153kHz

As reported in Figure 4-24, when rectifier current I_{S1} starts to decrease, a positive voltage caused by parasite inductance superpose with the resistive negative voltage and forced the total voltage to increase and cross the turn-off threshold too early. A phase lost of 900ns is detected and the MOSFET is not switched off at ZCS. The obtained phase lost is smaller than calculated (900ns vs. 1.4µs) because the secondary current waveform is not an ideal sinusoidal wave. The current increases slowly and decreases rapidly which shortens the phase lost duration.

The driving loss (gate charge loss) and conduction loss of each MOSFET can be calculated by the following formulas:

$$P_{dri} = U_{gs} Q_g f_{sw} \text{ (4-12)}$$

$$P_{c\_mos} = I^2{}_{rms\_FET} R_{dson} \text{ (4-13)}$$

Where Ugs is the driving voltage, I_{rms_FET} is the RMS current value of each FET die. The obtained driving loss is 0.73W per FET.

The power loss caused by phase lost (diode conduction) can be estimated as follows:

$$P_{c\_dio} = V_{SD} I_{Davg} f_s P \text{ (4-14)}$$

Where I_{Davg} is the average current of diode during this phase lost; V_{SD} is the forward voltage of the MOSFET's inverse diode; *f*s is the switching frequency; P is the phase lost duration. From the equation (4-14), diode conduction power loss of 14.6W is obtained for each LV MOSFET, which is even higher than the MOSFET conduction loss and should be reduced to obtain a high efficiency.

4.3.2 Proposed phase compensation scheme for synchronous rectification in LLC converters

As discussed in the above section, it is necessary to compensate the phase lost in synchronous rectification driving scheme for LLC resonant converters due to the LV MOSFET's series parasite inductance. Proposed solution for the prototype is to use a RDC filter to delay the voltage sense of Vds and compensate the phase lost with a time coefficient.

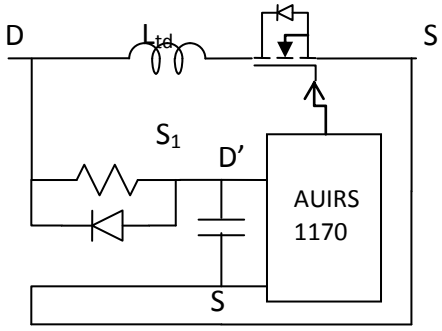


Figure 4-25. Proposed phase compensation scheme

The phase compensation scheme uses a RC filter to delay the measurement of Vds. At MOSFET turn-off, the Vd's measured waveform is delayed by the added RC filter by a time coefficient of ξ=RC. At the turn-on phase, a negative voltage is generated across drain-source of the MOSFET and this voltage turns the Schtokky diode D on instantaneously, which not delays the turn-on of MOSFET. Benefiting from the proposed phase compensation circuit, the MOSFET's switched off can be controlled by the filter's coefficient and the phase lost can be compensated. Figure 4-26 shows the compensation results by using R=150Ω, C=4.7nF.

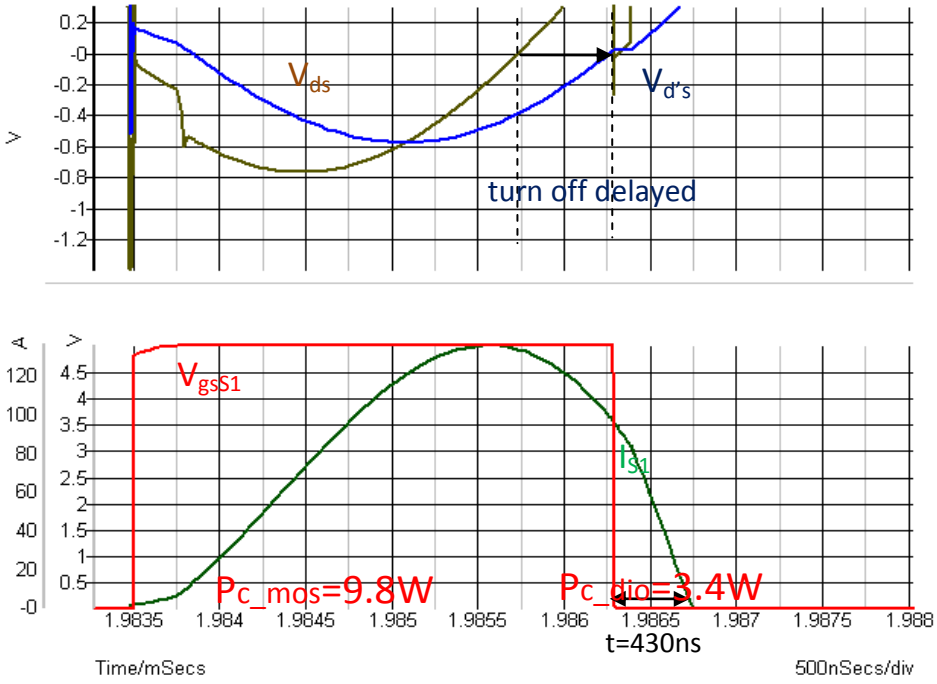


Figure 4-26. Phase compensation results by using R=150Ω, C=4.7nF

As reported by Figure 4-26, the measured Vd's is delayed compared to Vds which delays the MOSFET's turn-off. Phase lost is then reduced to 430ns. With lower current circulating the body-diode, the diode's conduction loss can then be reduced to 3.4W.

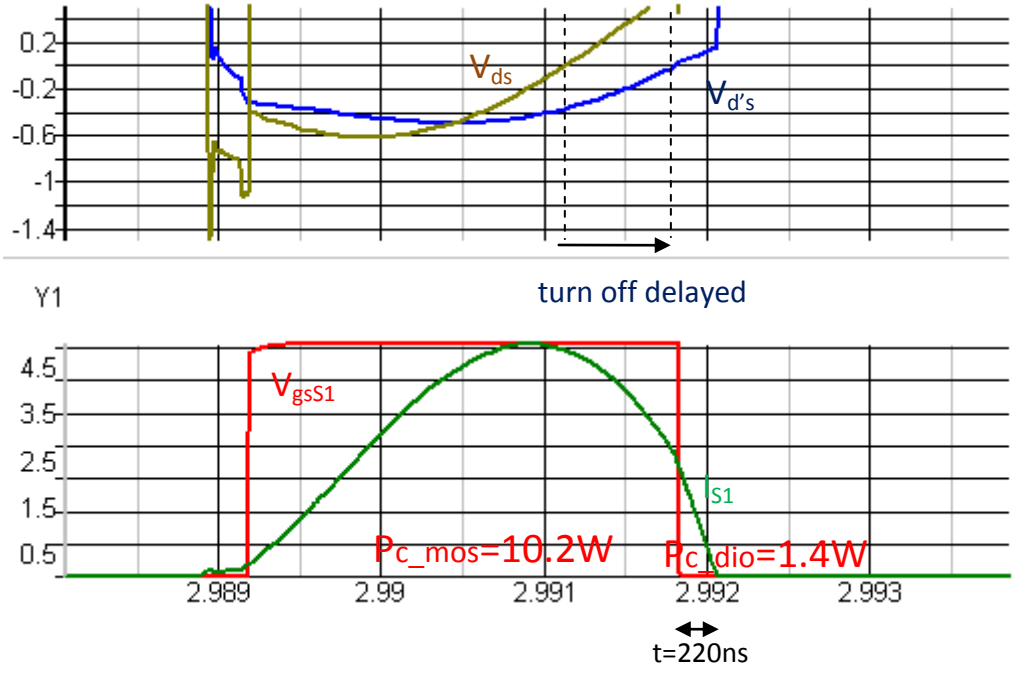


Figure 4-27. Phase compensation results by using R=220Ω, C=4.7nF

Figure 4-27 reports the phase compensation results by using R=220Ω, C=4.7nF. The phase lost is then reduced to 220ns and in this case, the switching loss is reduced to 1.4W. As shown in the above reported results, it is possible to fully compensate the phase difference by selecting a large time coefficient. However, for light load operation and high input voltage, switching frequency is increased and thus switching period is reduced. Moreover, at light load, the secondary current is low and the phase lost duration is also shorter (referring to Figure 4-23). Under this consistence, keeping a large time compensation coefficient risks in a late MOSFET turn-off then a reverse current circulates from the output capacitor back to the primary side (destroy the MOSFET easily). Thus in order to maintain a high efficiency for a wide load range, R=150Ω, C=4.7nF is the selected compromising solution.

4.3.3 Snubber design for voltage spike elimination

During the simulation analysis at the above section, the LV MOSFET's reverse recovery current is neglected. Due to large parasite inductance at transformer's secondary windings (~120nH), the diode's recovery current leads to a voltage spike across the MOSFET drain-source at switch-off. At low output current, the secondary current di/dt is low and this voltage spike is not significant, however, at high current, the reverse current becomes important and the Vds may exceed the avalanche voltage of MOSFET, which causes an additional power losses. Proposed solution to control this voltage spike is to implement a snubber at the IML terminals MOSFET level, shown as in the following circuit figure.

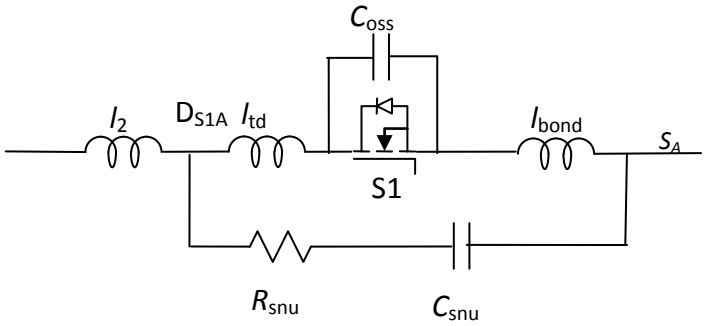


Figure 4-28. Proposed Snubber circuit to reduce the voltage spike (for switch S1)

In Figure 4-28, l_2 is the secondary wire leakage inductance; l_{td} and l_{bond} are the terminal parasite inductance and bonding inductance. Snubber power loss can be approximated by the following equation:

$$P_{snu} = C_{snu} V_{dspk}^2 f_s \quad (4\text{-}15)$$

In order to limit the power loss at each snubber to 2W, the Csnu should be limited to 5nF. The output capacitance for the selected MOSFET die is 4nF. A multi-step simulation is executed to find the optimal resistance Rsnu to attain the best damping, shown as in Figure 4-29.

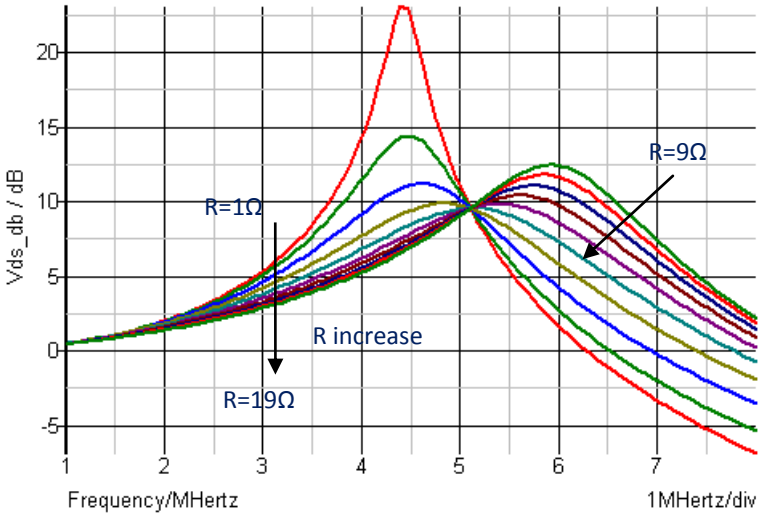
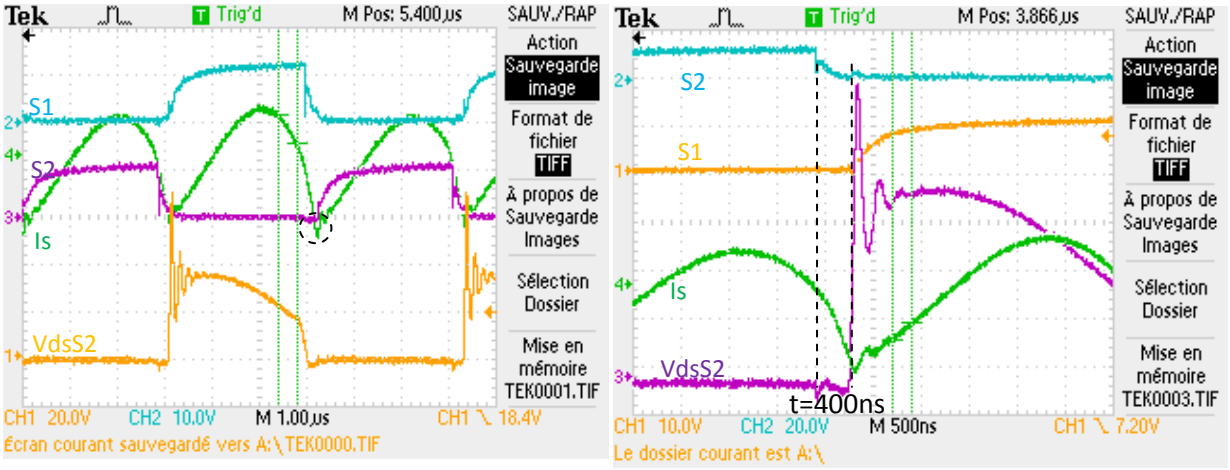


Figure 4-29. Damping characteristics by trying different resistance values

The voltage across MOSFET drain-source is measured in dB with sinus AC signal as simulated input. As reported by Figure 4-29, a snubber resistance Rsnu=9Ω permits to get the best resonant amplitude damping and is finally selected. Experimental results report the synchronous rectification results and voltage spike before and after damping:



(a) (b)

S1: 10V/div, S2: 10V/div, Is: 50A/div, V_{dsS2}: 20V/div in (a) and 10V/div in (b)

Figure 4-30. Phase compensated secondary waveforms without (a) and with snubber (b) (Vin= 330V, Iout=80A)

As reported in Figure 4-30, the switch-off signal arrive 400ns earlier than the current falls to zero, which is in accordance with the simulation results found in Figure 4-26 and verifies the proposed phase compensation circuit.

As reported in Figure 4-30 (a), the drain-source spike runs up to 70V (voltage clipped at 70V due to avalanche effect) without snubber. When a snubber is added, the drain-source voltage spike is reduced to 60V and the resonance is damped. The voltage clip phenomenon disappears.

The detected reverse-recovery time is trr=60ns and the maximum reverse current 10A. The switching loss due to reverse recovery current can be approximated by the following equation:

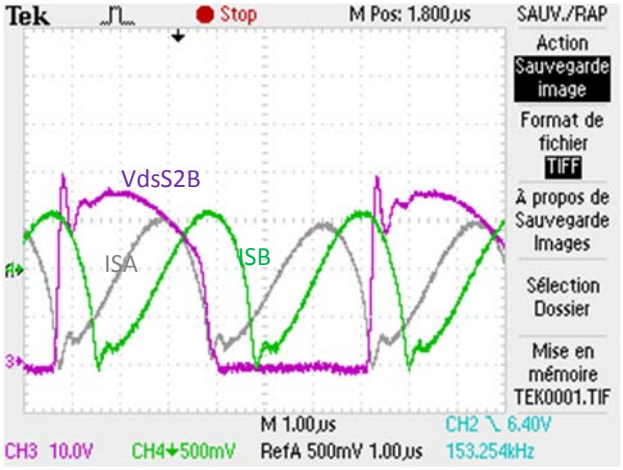
$$P_{rr} = -\frac{1}{Tsw}\int_0^{t_{rr}} \left(\frac{V_{pk}}{t_{rr}} t \left(\frac{I_{rpk}}{t_{rr}} t - I_{rpk} \right) \right) dt = \frac{1}{6} V_{pk} I_{rpk} t_{rr} f_{sw} \quad (4\text{-}16)$$

The obtained Psw is 1.5W for each MOSFET. The total power loss for each LV MOSFET is:

$$P_{MOS} = P_{dri} + Pc\_mos + Pc\_dio + P_{rr} \quad (4\text{-}17)$$

The total power loss for each MOSFET is 15.42W.

The following figure shows the output current sharing when both two power cells are on.



I_{SA}: 10A/div, I_{SB}: 10A/div, V_{dsS2B}: 10V/div

Figure 4-31. Current sharing result at Iout=40A, IA=IB=20A, Vin=330V

As reported at the above figure, the current is well distributed between the two power cells. The two power cells operate at different frequencies to keep the same output voltage and

share the same input current (A at 153.254 kHz, B at 154.812 kHz). It can be seen that at low output current, the MOSFET reverse recovery current is low and the drain-source is rather limited, compared to that of Figure 4-30.

4.3.4 Further discussion for practical applications

As discussed above, since the SR voltage measurement level is low, long wire connection introduces a parasite inductance and is susceptible to perturb MOSFET's command. Keeping the SR system robust is essential to the good operation of the whole resonant converter. A SR command failure at high output load often means a high diode conduction loss and risk to damage LV MOSFETs. Thus in practical applications, tasks should be done to get a robust SR system, make it less sensible to the parasite elements and external noises. In order to get a more robust SR and reduce connection length, a dedicated PCB is designed to connect directly on the modules, shown as in the following figure:

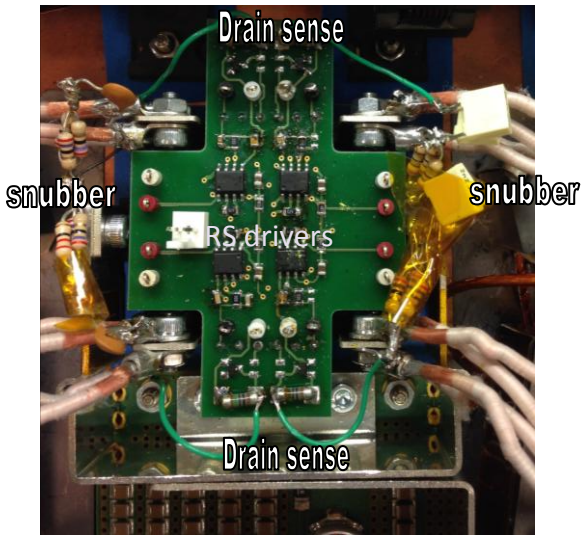


Figure 4-32. Practical ameliorations by a dedicated PCB board directly on the power module

As shown at the above figure, the designed synchronous rectification PCB is mounted directly on the signal connectors of IML power module and long wire connections are avoided. Four snubbers are connected to the drain terminals and source terminals. The drain voltage measurement is realized by a direct connection to the power module's drain terminal. Experimental results among all the power load range prove that this SR arrangement achieves a correct and robust operation.

4.4 Air cooling system and prototype assembly

4.4.1 Vapor chamber as a new solution for air cooling in automotive DCDC converters

As power electronic devices decreases in size and increases in power, the thermal management is a key for power applications. One challenge of the actual designed LLC resonant converter is the ability to implement an innovative cooling solution. As for air cooling solution, standard aluminum extrusions no longer have the capacity to sufficiently spread the power losses generated by electronic components and hot points exist. The cooling solution adopted here is by inserting a vapor chamber into the base of the heat sink, shown as in the Figure 4-33.

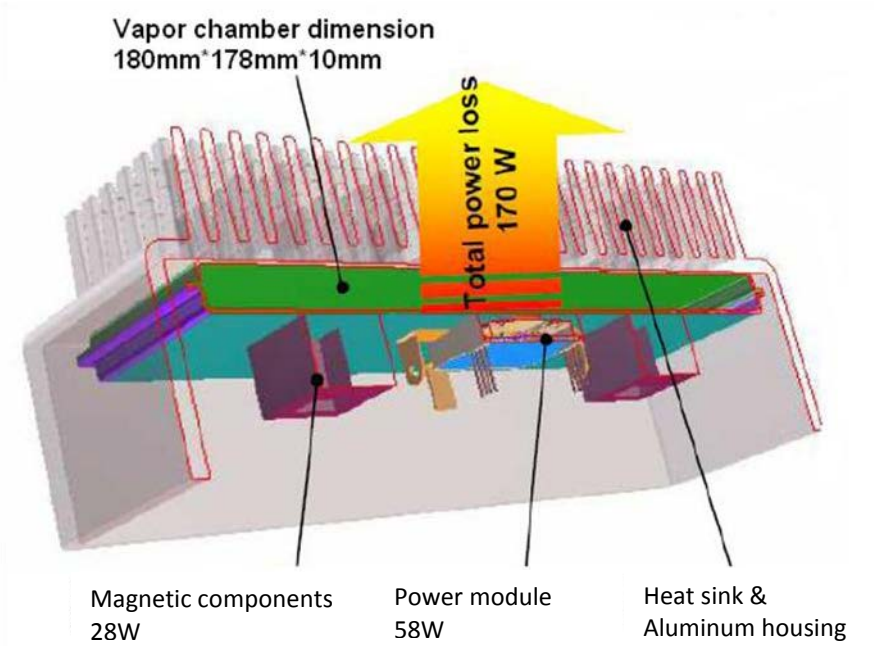


Figure 4-33. Insertion of a vapor chamber into the base of the heat sink for cooling

The principle of vapor chambers is explained as follows [4-20, 4-21]: Vapor chambers are essentially flat or planar heat pipes that use the principles of evaporation and condensation to produce a heat spreading device with a very high conductivity thermal plane. Like traditional cylindrical heat pipes, heat is evacuated using internal wick structure and a working fluid, assuring a uniform temperature distribution and an elimination of hot spots, as shown in Figure 4-34:

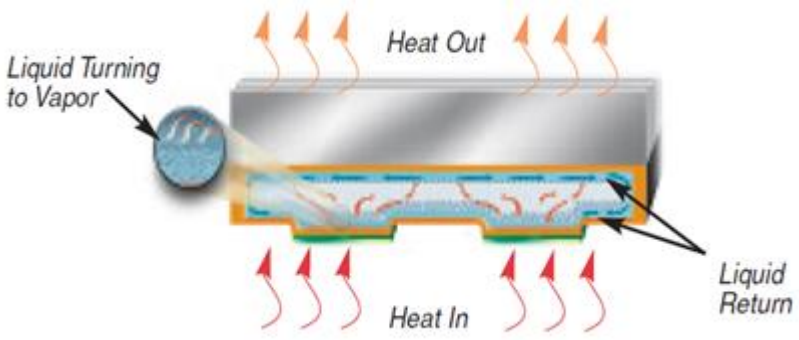


Figure 4-34. Principles of vapor chambers for heat spreading

The wick is saturated with a working fluid. At the location where the heat is produced, the fluid immediately vaporizes and the vapor rushes to fill the vacuum. Once the vapor comes into contact with a cooler surface it condenses, releasing its latent heat of vaporization. The condensed fluid returns to the heat source via capillary action at the wick, ready to be vaporized again and the cycle continues. Furthermore, the capillary action enables the vapor chamber to work in any orientation effectively with respect to gravity. Physically, the vapor chamber enables to better distribute the heat among its total surface. The most common combination in the electronics cooling field is copper and water due to the LLC converter's operating temperature in automotive use.

Experimental and simulation are done in order to study the effectiveness of vapor chamber compared to a copper plate as heat spreader. The experiment is shown in Figure 4-35.

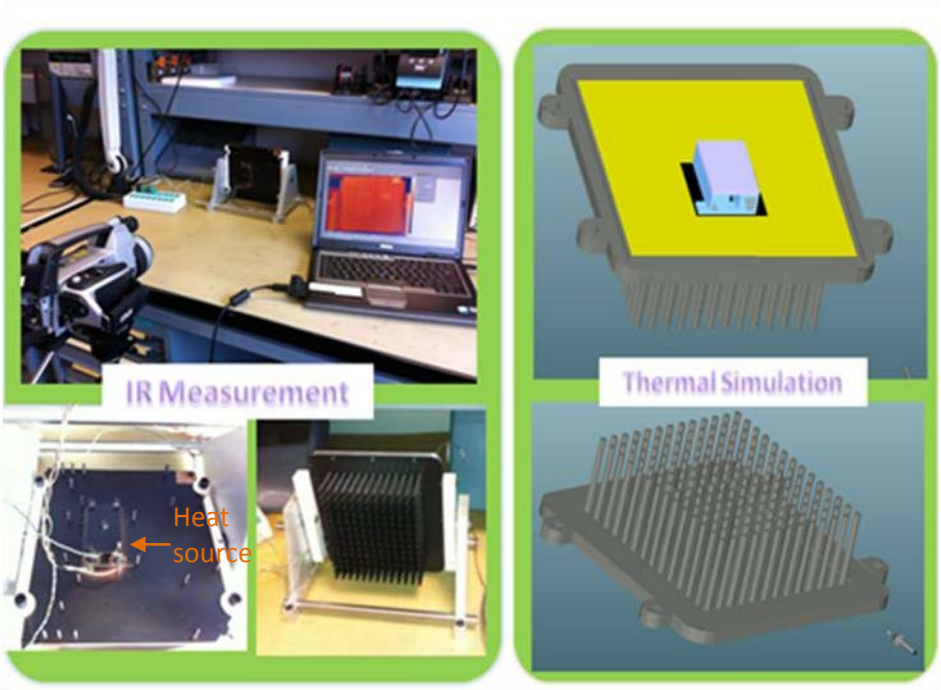


Figure 4-35. Experiment and simulation set-up for vapor chamber study

Heat source of 58W (to simulate the heat generated by LV power module) is produced by two power resistors of 29W each. An infra-red camera (IR camera) and a laptop are used to record temperature information from experiment. In order to make a precise temperature measurement, the vapor chambers and fin heat sinks are painted to black. Three scenarios are considered in this experiment: one with copper plate (with same dimension as vapor chamber) as heat spreader, one with vapor chamber as heat spreader, the last one with vapor chamber and heat sink. Thermal simulation is modeled and conducted by computational fluid dynamics (CFD) software. The obtained results are shown in Figure 4-36.

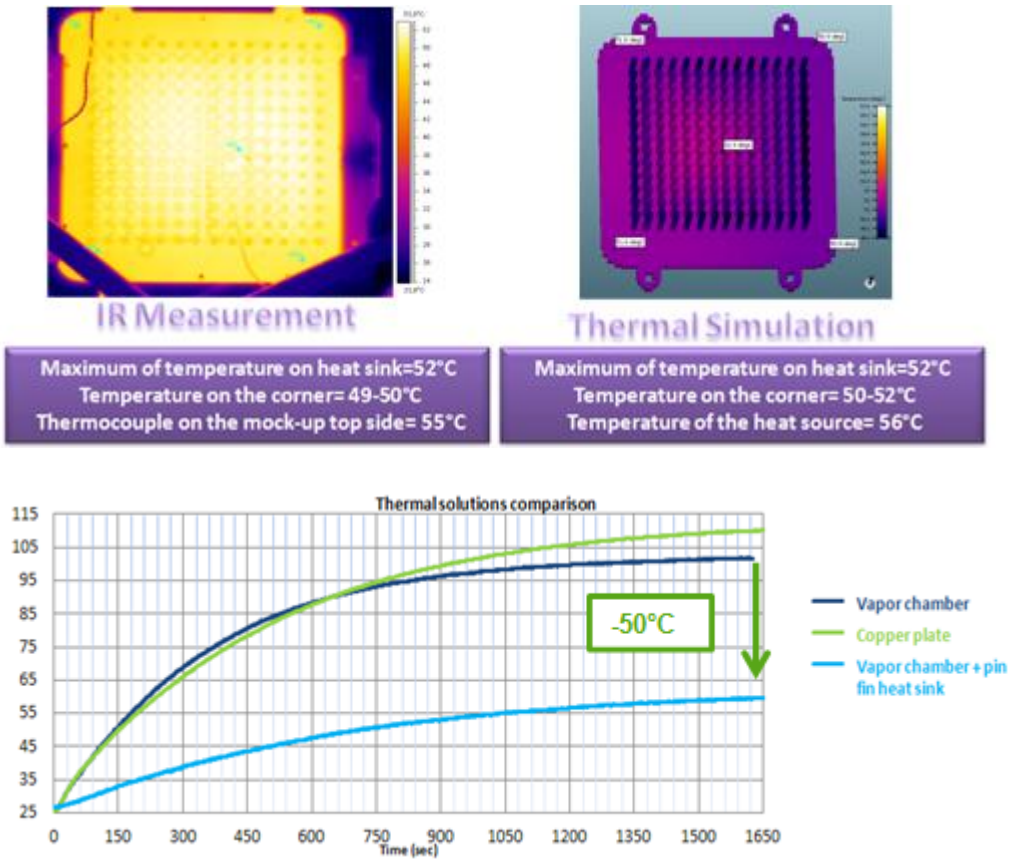


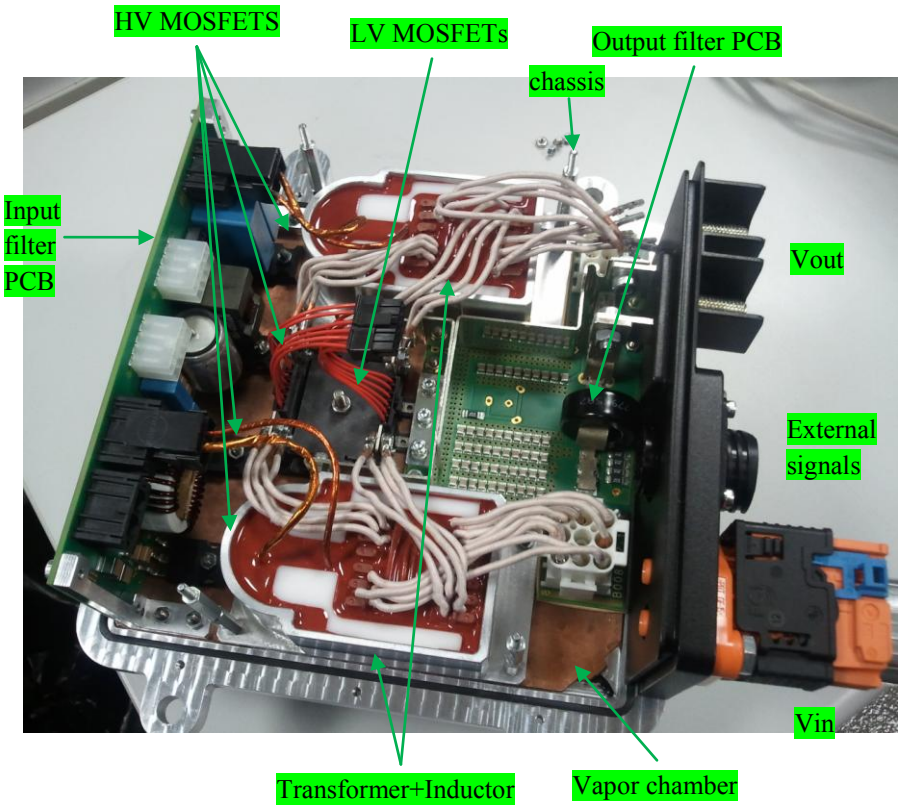
Figure 4-36. Experimental and simulation results for vapor chamber study

Results find that there is a good correlation between the experimental results and simulation results. The thermocouple at the heat source extracts a temperature at 55°C, while the simulation is at 56°C. The maximum of temperature on the heat sink is observed at 52°C during the measurements and also in the simulation. Results also find that the vapor chamber alone is a little more effective than a copper plate (with same dimension) a few degrees (~ -

10°C). Moreover, the vapor chamber associated with the pin fin heat sink is much more efficient (~ -50°C).

4.4.2 Prototype assembly and cooling system performance

The following picture shows the components integration within the prototype. As the input filter PCB's power loss is rather limited, it is mounted vertically to reduce the overall volume. HV MOSFETs are placed at the bottom of the input filter PCB, and they are mounted directly to the vapor chamber and fixed by screws to improve the cooling effect. Thermal interfaces are needed to isolate the HV MOSFETs from the vapor chamber. Magnetic components, LV MOSFETs modules are mounted also on the vapor chamber directly. Here, the long wires of IML can be replaced by a dedicated PCB shown in Figure 4-32. The control board is mounted on top of the transformer with a 4-leg support. One spacer connects the chassis ground to the control PCB board. The control PCB board is mounted on the four spacers, above the power components. An external connection with 16 lines is used for exchanging control signals and export measurement results. After assembly, the prototype performs an overall volume of 2.5L, 3kg and 2.5kW nominal power (3kW peak power). The power density is 1W/cm^3.



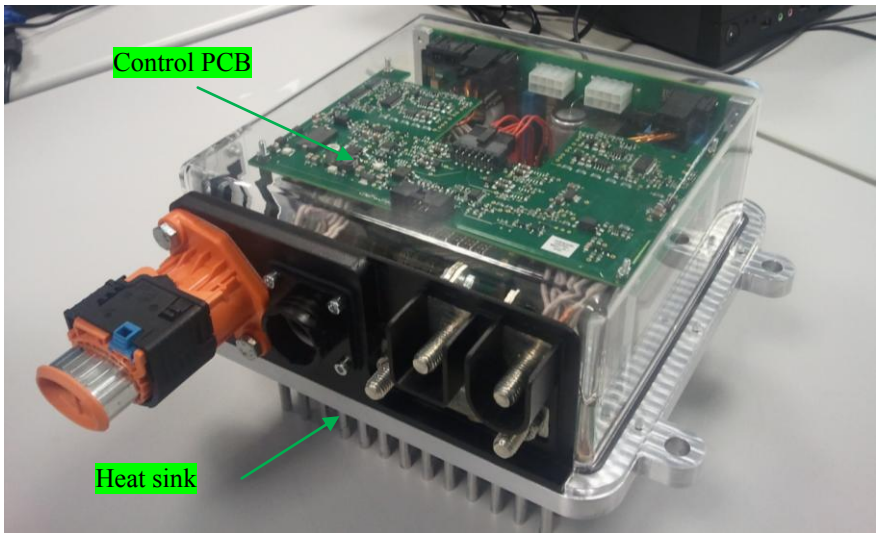


Figure 4-37. Prototype assembly of LLC converter, power density 1W/cm3

Experiments are made to test the effectiveness of cooling system integration and system assembly, with experimental results shown as follows:

Table 4-4. Experimental results of the cooling system's thermal characteristics with the prototype

Heat spreader	Heat load (W)	Ambient (°C)	Orientation	ΔT_{XY}	ΔT_Z	Tmax at vapour chamber
Copper plate	150	22°C room	Horizontal	16°C	10°C	101°C
Vapor chamber	150	22°C room	Horizontal	4°C	7°C	84°C
Vapor chamber	150	-20°C oven	Horizontal	25°C	0,5°C	28°C
Vapor chamber	150	0°C oven	Horizontal	19°C	1°C	46°C
Vapor chamber	150	70°C oven	Horizontal	4°C	11°C	119°C
Vapor chamber	150	70°C oven	Vertical	3°C	13°C	123°C

Where ΔT_{XY} stands for temperature difference along the vapor chamber flat surface, and the ΔT_Z stands for the temperature difference along vertical axis.

As reported in the Table 4-4, vapor chamber is more efficient in spreading heat equally among its flat surface than a copper plate, with a ΔT_{XY}=4℃ compared to ΔT_{XY}=16°C under 22°C ambient. As temperature decreases, its ability in spreading heat among XY surface is decreased (with ΔT_{XY}=19℃ at 0℃ oven and ΔT_{XY}=25℃ at -20℃ oven). At ambient temperature -20℃ , 0℃ and 22℃ , the maximum temperatures are all maintained less than 105℃ (maximum authorized at specification). As ambient temperature increases to 70℃ , the maximum temperature attains 119℃ . It is also found that there are no significant differences from horizontal to vertical orientation (~ +4℃), which in turn verifies the vapor chamber's solid effectiveness regardless of its real orientation in practical use, which is an ideal solution for electric/hybrid vehicle manufacturers to arrange it in any orientation inside the cars.

As shown in Table 4.4, under an ambient temperature 70℃ , the maximum temperature attains 119℃ , which exceeds the upper limit of 105℃ defined for components internal environment. In this case, the converter needs to be further cooled by external forced air convections. Figure 4-38 shows the simulation results with forced air-convection 1.5m/s under CFD analysis.

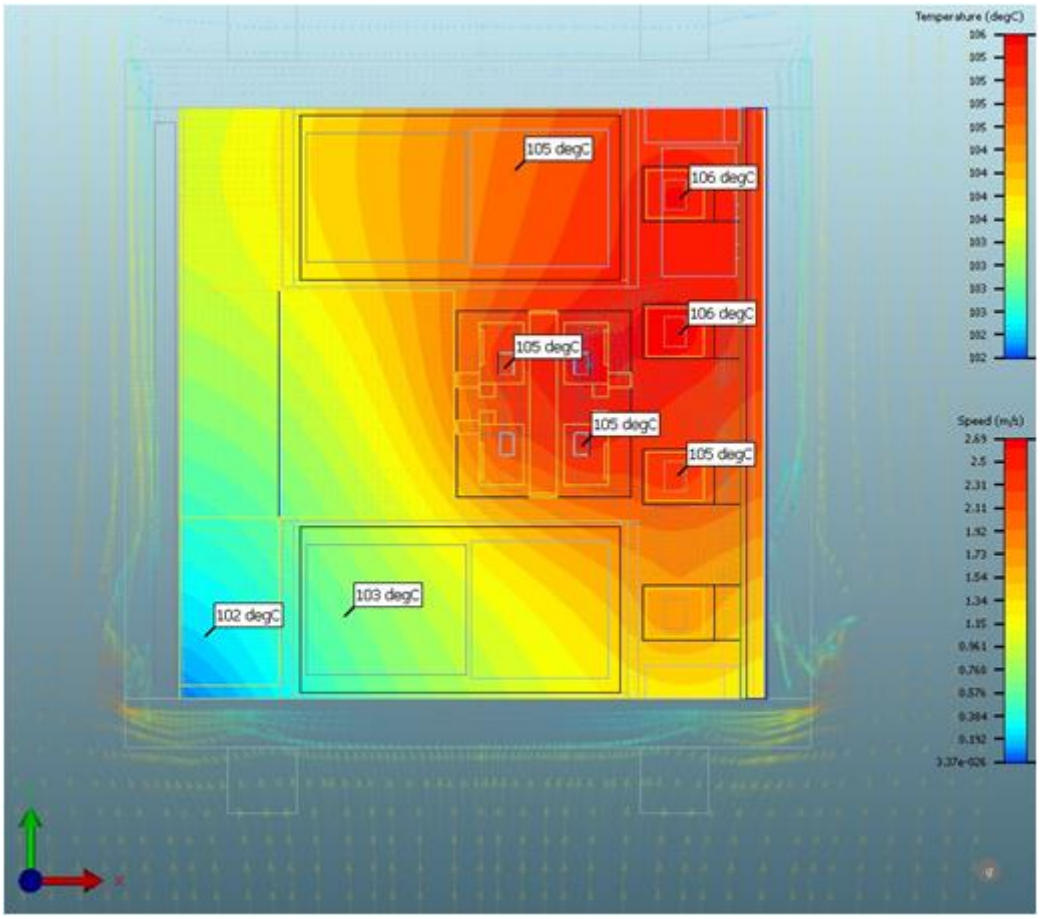


Figure 4-38. Simulation results of temperature rise at nominal power with a forced air-convection 1.5m/s at ambient 70℃

As shown in Figure 4-38, the internal temperature is maintained less than or around 105℃ and ΔT_{XY}=4℃ . The proposed prototype can be used at room temperature without air convection and at 70℃ with forced air convection to get a better cooling effect.

After careful prototype assembly and cooling system design, a small size, high efficiency, and high power density LLC converter prototype is obtained. Experimental verifies that using vapor chambers can be an efficient way to manage heat in LLC converter design and implementations, where effective cooling helps ensure long component life and high reliability.

4.5 *Efficiency and power loss analysis*

The most important aspect of this designed LLC converter is its performance in conversion efficiency. The designed test bench for converter's operation and efficiency measurement is shown as follows:

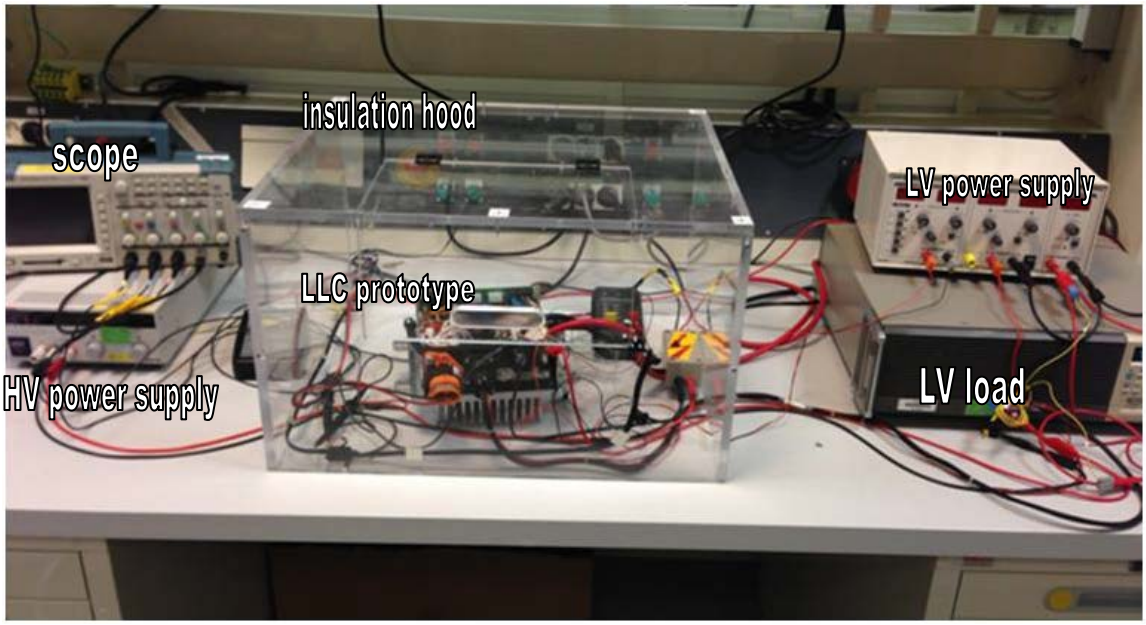


Figure 4-39. Test bench of designed LLC converter prototype

Efficiency has been measured for the power cell A, power cell B and for the two power cells operating in parallel together. Figure 4-40 shows the measurement efficiency result for Vin=330V; Figure 4-41 shows the measurement efficiency result for Vin=410V.

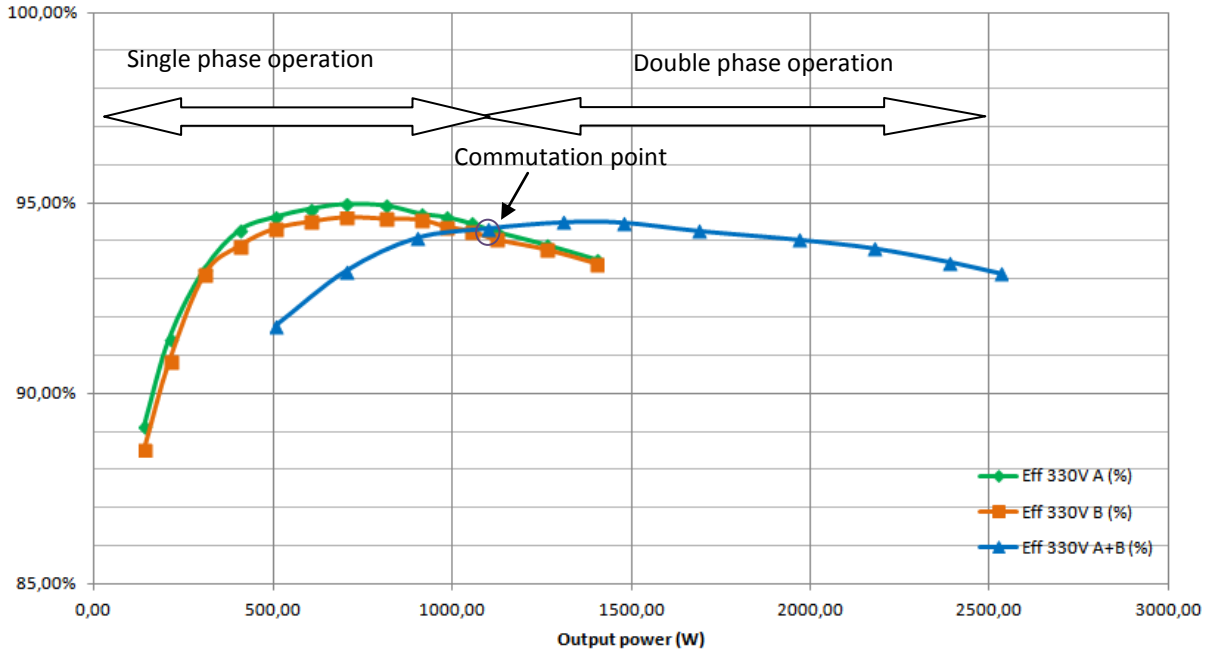


Figure 4-40. Measured efficiency result for Vin=330V

As reported in Figure 4-40, the conversion efficiency of a single cell LLC converter is maximal at 700W, with a peak efficiency of 95% for phase A and 94.7% for phase B. Due to the component dispersions, the performance of these two power cells is slightly different. Efficiency begins to decrease when load power exceeds 700W. Setting P=1.1kW as the boundary for single cell operation and double cell operation is a good choice to keep a high efficiency over a high output power range. When output current exceeds 1.1kW, both the two cells operate and efficiency continues to increase from 1.1kW to 1.5kW.

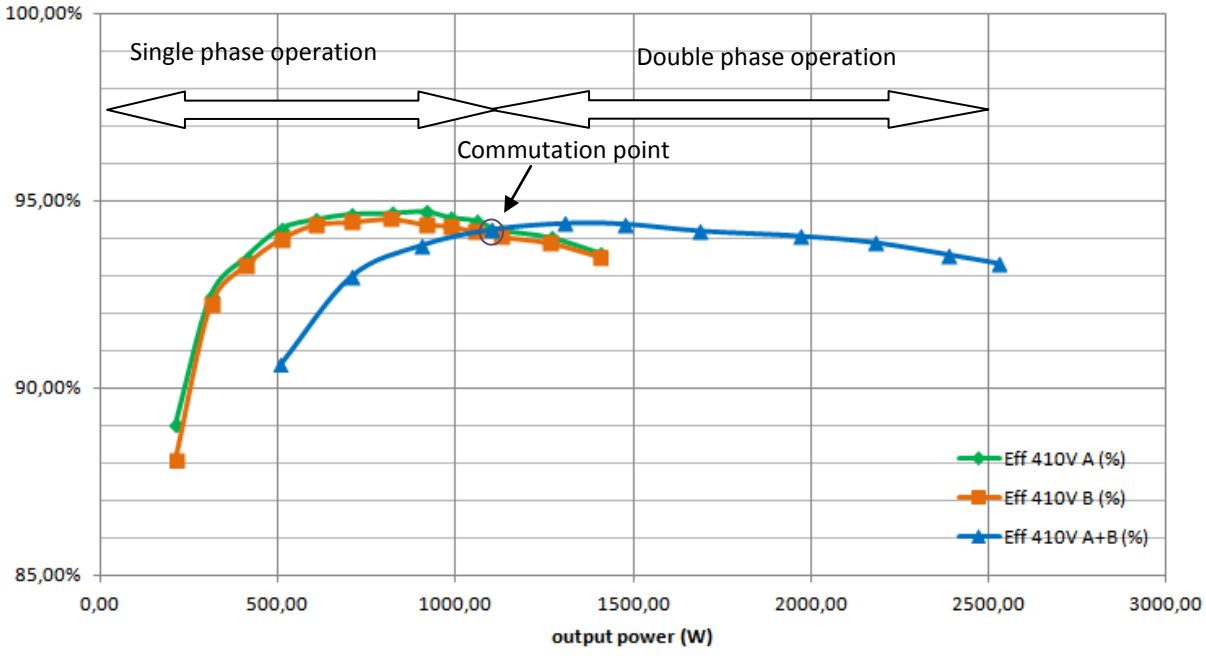


Figure 4-41. Measured efficiency result for Vin=410V

At 410V, the converter operates at a higher switching frequency, which increases all the ac resistances but decreases its primary current. These two effects balance the overall power loss. The overall power efficiency result is similar to that of 330V, with a peak efficiency at 410V slightly reduced to 94.7% instead of 95%. In all, the designed double phase LLC converter exhibits very good conversion efficiency at a large load variation range: Efficiency >94% from 500W to 2kW; Efficiency>93% from 300W to 2.5kW. Even at very low load (150W), the conversion efficiency is around 90%. The obtained conversion efficiency is far higher than the specified efficiency 92% described at the beginning of this project.

The loss breakdown of the proposed 2.5kW, 250kHz, HV/LV LLC resonant converter is shown in the following two tables. The calculations are in good agreement with the experimental results.

Table 4-5. Calculated loss breakdown of the designed LLC converter at 800W, Vin=330V (single cell operation)

Description	Types	Values
Primary MOSFET	Conduction loss	1.58W
	Gate loss	0.60W
	Switching loss	~0W
	Total loss (x2)	*4.36W*
Secondary MOSFET	Driving loss	0.72W
	FET Conduction loss	4.0W
	Diode conduction loss	1.5W
	Reverse recovery loss	0.7W
	Total loss (x2)	*13.84W*
Inductor	Core loss	0.85W
	Copper loss	0.90W
	Total Loss (x1)	*1.75W*
Transformer	Primary copper loss	1.8W
	Primary Eddy current loss	1.5W
	Secondary copper loss	6W
	Total copper loss	9.3W
	Core loss	8.4W
	Total loss (x1)	*17.7W*
Input filter	Conduction loss	*0.20W*
Output filter	Conduction loss	*0.44W*
Snubber	Conduction loss	*4.00W*

RS filter	Conduction loss	*2.65W*
fuse	Conduction loss	*0.81W*
Total	Total Loss	*45.75W*
Efficiency (driver included)		*94.6%*
Efficiency		*94.9%*

Table 4-6. Calculated loss breakdown of the designed LLC converter at 2.5kW, Vin=330V (Double cell operation)

Description	Types	Values
Primary MOSFET	Conduction loss	3.43W
	Gate loss	0.60W
	Switching loss	~0W
	Total loss (x4)	*16.12W*
Secondary MOSFET	Driving loss	0.72W
	FET Conduction loss	9.8W
	Diode conduction loss	3.4W
	Reverse recovery loss	1.5W
	Total loss (x4)	*61.68W*
Inductor	Core loss	1.85W
	Copper loss	1.96W
	Total Loss (x2)	*7.62W*
Transformer	Primary copper loss	3.92W
	Primary Eddy current loss	1.5W
	Secondary copper loss	14.7W
	Total copper loss	20.12W
	Core loss	8.4W
	Total loss (x2)	*56.24W*
Input filter	Conduction loss	*2.20W*
Output filter	Conduction loss	*4.20W*
Snubber	Conduction loss	*8.00W*
RS filter	Conduction loss	*5.33W*
fuse	Conduction loss	*10W*
Total	Total Loss	*171.39W*
Efficiency(driver included)		*93.5%*
Efficiency		*93.7%*

In the chapter 2, we proved that in order to broaden the input voltage range of the designed LLC converter, adopting a BOOST converter at the input stage of the LLC is a sensible

solution instead of setting a low magnetizing inductance value Lm, while the latter causes higher reactive circulating currents and even worse efficiency. Under this case, a BOOST converter is needed to increase the voltage level from 220-330V to 330V. High voltage BOOST converter with very high efficiency (98.7%-98.4% estimated) is easy to be designed. In order to validate this proposal, we adopt the transformer with Lm=24μH (e=3.96mm) described at the part 4.2.3 into the same converter prototype and compare its efficiency by experiment. Comparison is made for two cases: single stage LLC with Lm=24uH, Vin=220V and double stage BOOST+LLC with Lm=42uH, Vin=220V. Experiments are executed for operation of single cell "A" until 1.5kW.

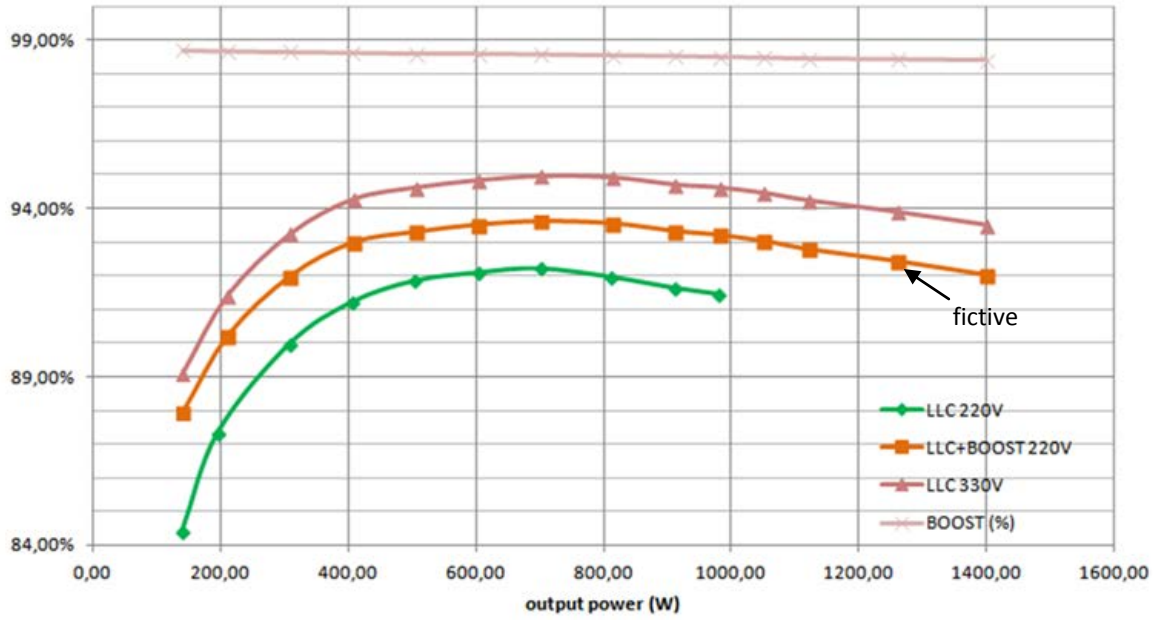


Figure 4-42. An efficiency comparison of single stage LLC and double stage BOOST+LLC

Based on the measured efficiency curve of single stage LLC, the double stage LLC's efficiency can be predicted and a fictive efficiency curve is plotted. This fictive curve includes the efficiency prediction of a BOOST PFC from 220V to 330V and a LLC from 330V to14V. As reported at the above figure, although double stage LLC includes extra loss from the PFC, its overall conversion efficiency is still at least 1% higher than single stage LLC. Single stage LLC with Lm=24uH results in a poor power factor (primary rms current increased from 13A to 18A due to high circulating magnetizing current), which doubles the primary conduction loss and the inductor core loss. Furthermore, the transformer's air-gap is increased from 1.98mm to 3.96mm, causing 4.3W more eddy current loss at each transformer.

For double stage LLC, when input voltage is higher than 330V, the BOOST converter is inhibited and there is only a slight diode voltage drop at the input stage, the conversion efficiency will not be influenced. In all, double stage BOOST+LLC is a more suitable candidate solution for improving the voltage regulation range other than single stage LLC.

4.6 References

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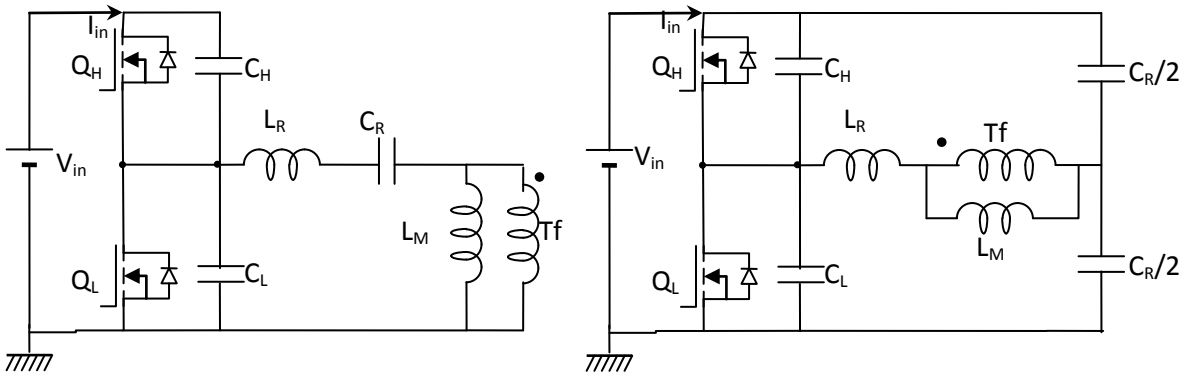
Chapter 5. Electromagnetic Compatibility Analysis of Double Phase LLC

5.1 Improvement of double phase LLC for conducted emission reduction

5.1.1 LLC cell arrangement

There are two different ways of arranging a LLC resonant cell. A traditional way is keeping a separate resonant capacitor, as that shown in Figure 5-1(a). Another way is to divide the resonant capacitor into two capacitors in parallel and arrange them as that shown in Figure 5-1(b).



(a) (b)

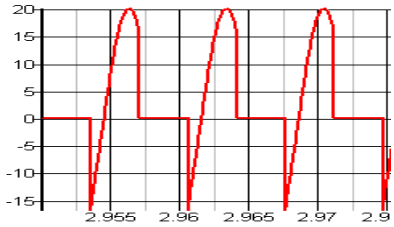
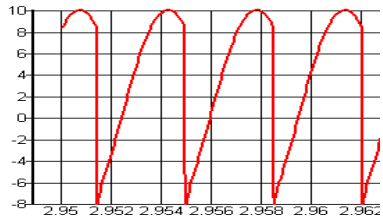
Figure 5-1. Two different ways of arranging the LLC power cell

The two different power cell arrangements neither change the circuit principle, nor the circuit operation. However, the structure (b) is highly preferred than structure (a) in the aspects of differential mode conducted emission reduction.

In the structure (a), the input current injected to the power source equals to the current passing through the MOSFET Q_H and the capacitor C_H. Q_H is switched on for half a period and switched off for another half period, thus the input current is a rectified half sinus waveform (with some phase difference as the power factor is less than 1), as that shown in the Table 5.1. The main noise is at its switching frequency, 174dBμV at *fs*=153kHz. Another important noise is at at 2*fs*, with 170dBμV. As in the structure (b), the resonant current is split equally to two currents flowing through two half resonant capacitors. The input current is thus the sum of the half resonant current and the current of Q_H, which is a rectified full sinus wave (also with some phase difference as the power factor is less than 1), shown as in Table 5-1. The

basic noise is at 2*fs*, 171 dBμV. In conclusion, the structure (b) eliminates all the 2k-1 harmonic noises. Furthermore, the basic noise frequency can be doubled without doubling the switching frequency. The converter can be operated at 150-250kHz to get a targeted emission range from 300-500kHz. Of course, the structure (b) is a better candidate than structure (a) for noise reduction and is the final solution adopted in this project.

Table 5-1. Comparison of conducted emissions for circuit structure (a) and (b)

	Structure (a)		Structure (b)	
Iin current waveform				
Main noise at	*fs*		2**fs*	
Primary harmonics at	Iin	V_{LISN}	Iin	V_{LISN}
fs	20dBA	174dBμV	~	~
2*fs*	16dBA	170dBμV	17dBA	171dBμV
3*fs*	-17dBA	137dBμV	~	~
4*fs*	7dBA	161dBμV	8dBA	162dBμV
5*fs*	-23dBA	131dBμV	~	~
Good candidate?	No		Yes	

At the secondary side, the two structures have no difference in views of conducted noise.

Table 5-2. Conducted emissions for at the secondary sides

Secondary harmonics at	Io	V_{LISN}
fs	~	~
2*fs*	35dBA	189dBμV
3*fs*	~	~
4*fs*	21dBA	175dBμV
5*fs*	~	~

5.1.2 EMC discussion of double phase LLC

In the designed double phase LLC resonant converter, slight variations and component mismatches among different cells generate small differences in their operating frequencies.

The interaction between the switching noises of each resonant cell creates the undesired beat frequencies, at multiples of the differences between their operating frequencies. Very few literatures report this phenomenon: the reference [5-1] has proposed a signal sampling-recovery model for calculating the beat frequency and its amplitude in a BUCK converter under the condition that the input voltage is with high frequency interference. The reference [5-2] prompts it to the applications of multi-phase Buck converters. In parallel-parallel LLC converter, the case is different.

From the considerations of designing simplicity and component sizes minimization, both the two power cells share the same input filter, the only filtering between the two cells is the decoupling capacitors C1 and C2. Because of different switching frequencies of the two power cells, their ac input ripple current frequencies are also different. With a common input and no inductive filtering, the ac ripple current from the cell (a) generate voltage ripples *v*a with 2*f*a at the input of cell (b). Shown as in the following figure:

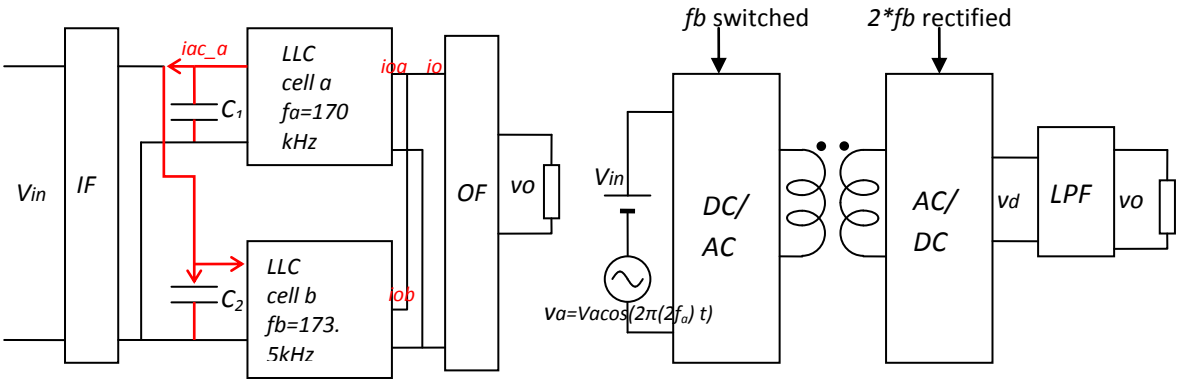


Figure 5-2. Circulating ac current from the phase (a) to phase (b) and a model for beat frequency analysis

Firstly, let's start at considering the influence of the phase (a) to the phase (b), referring to Figure 5-2. The ripple current of the phase (a) at frequency 2*f*a develops an ac voltage at the bypass capacitor C_2 with an amplitude Va. This ac voltage adds up with Vin as the input voltage of the phase (b). By LLC half bridge switching and center-tapped rectifying, an amplitude modulation is generated at 2 times of the switching frequency of phase (b): 2*f*b. Low frequency (LF) component at 2(*f*b-*f*a) appears at the output side. Moreover, considering a mutual interference between phase (a) and phase (b) by circulating ac current, this LF beating also appears at the input side; the corresponding spectrums and waveforms are shown in

Figure 5-3. As the two frequencies are close to each other, this LF beating noise may not be sufficiently attenuated by the LP filter.

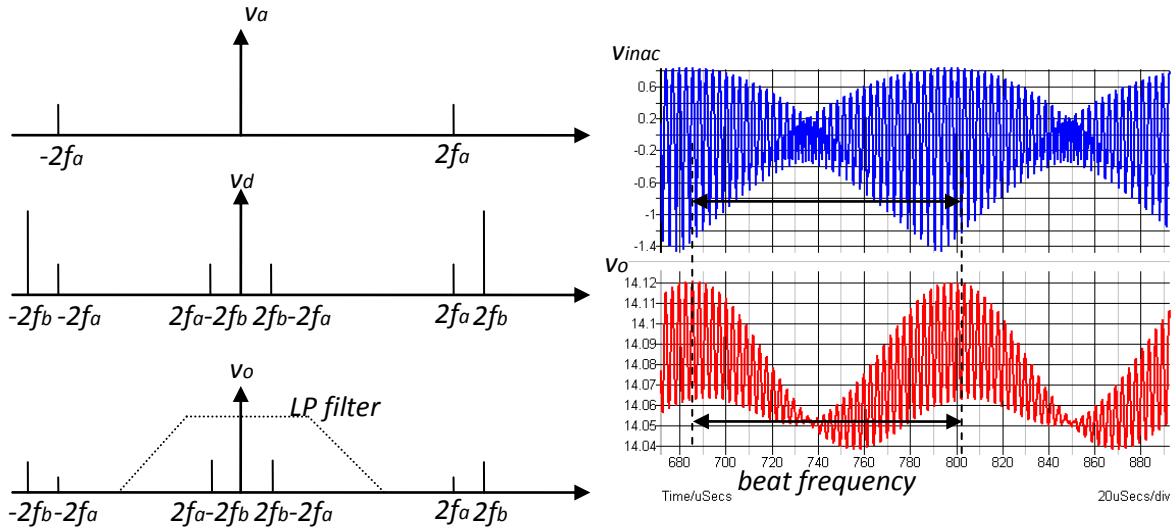


Figure 5-3. Illustration of beat frequency at low frequency domain of double cell LLC

High additive ripple currents can stress input bypassing capacitors and system noise can be increased, depending on the board layout. In some cases, these circulating currents can interfere constructively with sufficient amplitude to lead to converter's unpredictable behavior [5-3]. To damp this LF beating, sufficient bypass capacitors are necessary at the input of each power cell to reduce the voltage level of *va*. If LF beating is still important, one can series connect an inductor for each power cell to inhibit the circulating ac current. Shown as in Figure 5-3, the input ripple voltage is rather limited by properly choosing the bypass capacitor value.

Furthermore, input and output filters should not contain any resonant points at low frequency range; if not, this ripple may be amplified by the filters and is harmful to the stable operation of LLC resonant converter. Thus the filter's gain should be precisely designed and controlled.

At high frequency, the EMC plot of each cell's input/output current shows the main noises at 2*f*a and 2*f*b. A sum of two currents results in a superposition of noises at the frequency domain, as shown in Figure 5-4.

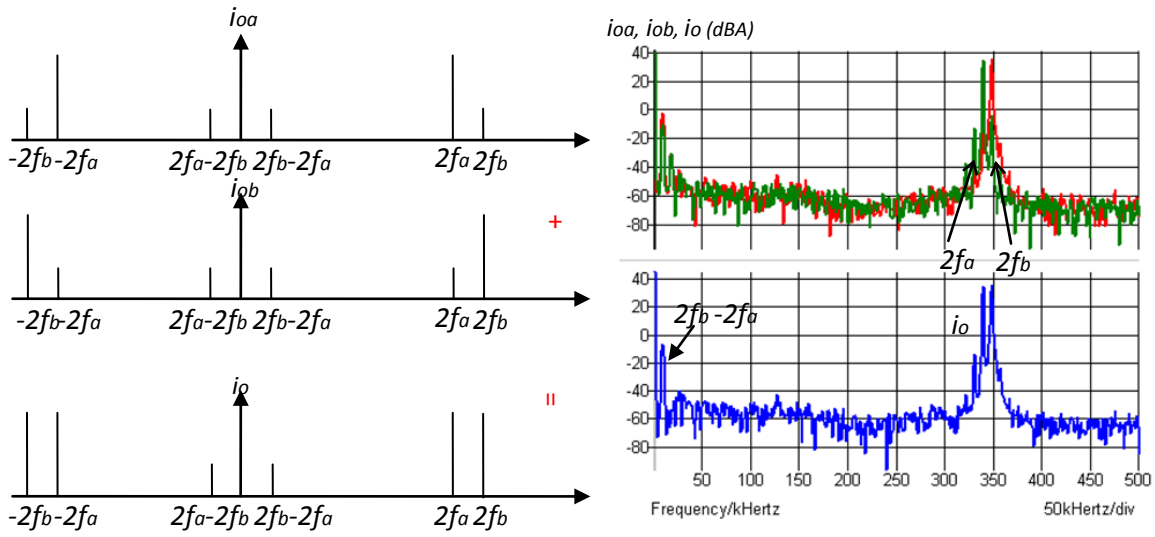


Figure 5-4. Superposition of two output currents in frequency domain

After superposition, the noise at one phase's output current superpose with the noise of other phase whose noise frequency is slightly different. One can design the input/output filters based on the conducted noise levels of one phase, the other phase benefits naturally the same attenuation at the adjacent frequency. Compared with one single LLC cell at 2.5kW, double phase LLC benefits a 6dB noise level reduction at both input/output sides. This is one great advantages of the proposed double phase LLC.

5.2 Filter Design and Improvement

5.2.1 Input Filter Design and Dimensioning

The adopted filter topology as input filter is the PI (Π) filter, shown as in Figure 5-5.

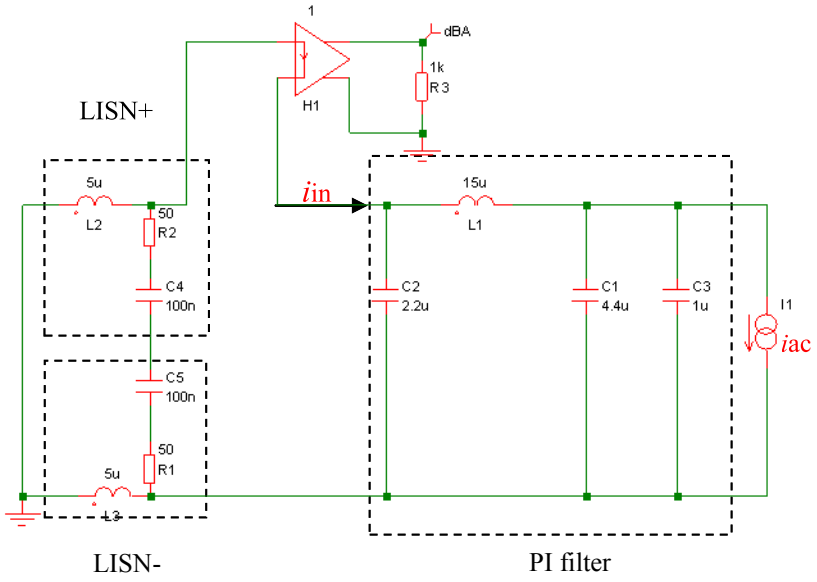


Figure 5-5. Basic topology of PI filter as input filter for DM noise filtering

At the targeted high noise frequency, ωL2<50Ω, the PI filter (also written as Π filter) can be considered a fourth order filter composed by two 2nd order LC filters: L2+L3 and C2, L1 and C1//C3. L2 and L3 are the line inductances of the line impedance stabilization network LISN+ and LISN-, separately. The filter's attenuation at the targeted noise frequency can be approximated by the following equation:

$$Gain = \frac{i_{in}}{i_{AC}} = \frac{1}{2 \cdot L1 \cdot L2 \cdot (C1 + C3) \cdot C2 \cdot s^4} \quad (5\text{-}1)$$

With $L_1\omega >> 1/(C_2+C_3)\,\omega$, $2L_2\omega >> 1/C_2\omega$ at $\omega = 2\pi(2fs)$. The inductor and capacitor values are selected according to the targeted gain requirements at the switching frequency range. C3 capacitor of 1uF corresponds to the 470nF local decoupling capacitor added to each cell. At the designed PI filter, two resonances exist: L2+L3 is resonant with C2 at f_{l1}= 36kHz and L1 is resonant with C1//C3 at f_{l2}=17kHz. As described at the above section, resonances at low frequencies may cause unpredictable behavior to the parallel operation of LLC resonant cells and should be properly damped. The following figure proposed a well damped version of the PI filter:

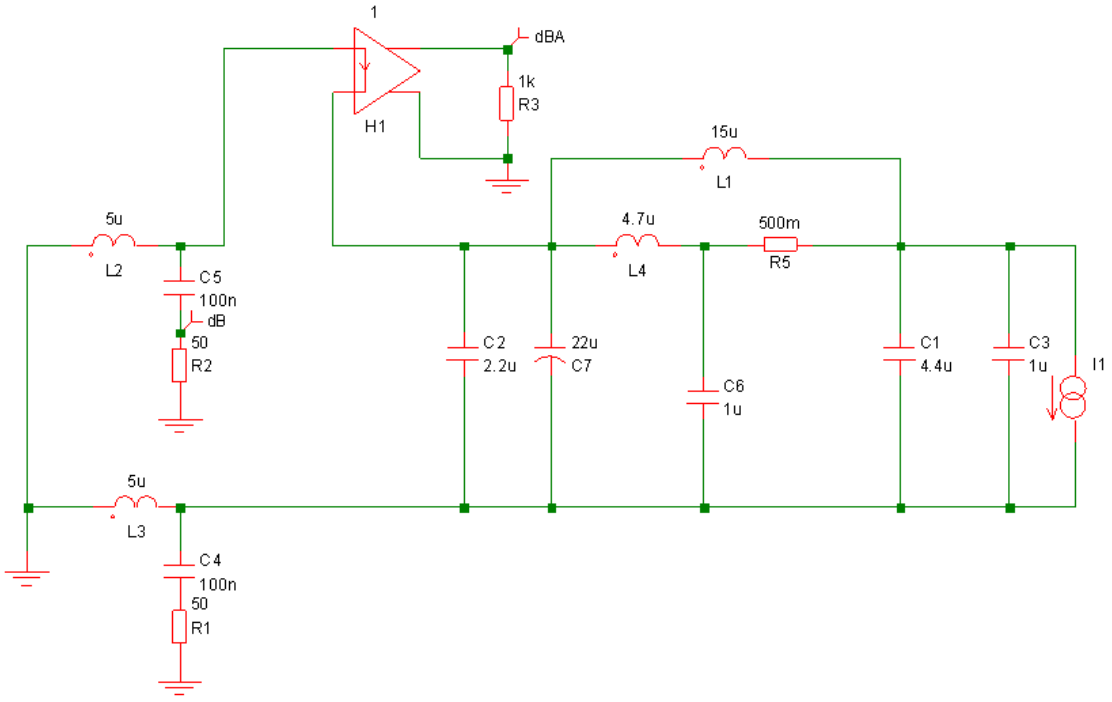


Figure 5-6. Damped version of proposed PI filter

To damp the resonance at f_{l1}, an electrolytic capacitor C7 is placed across C2. The capacitor C7 and its internal resistance serve as a gain attenuator. To damp the resonance at f_{l2}, L4 and R5 are added. C6 is implemented to reduce the impedance of the parallel path connected across L1 which reduce the filter gain at higher frequency. A further resonance introduced by L4 and C6 is damped by R5 and C1. The filter's performances before damping and after damping are compared at the following figure.

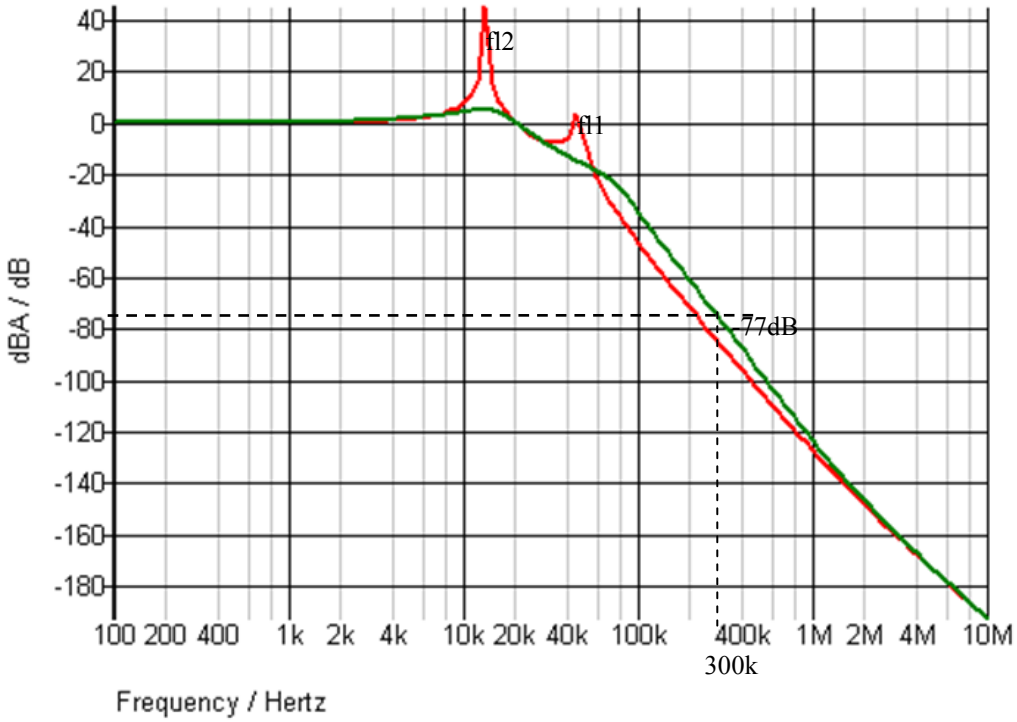


Figure 5-7. Filter's gain before (red) and after (green) damping

As shown at the above figure, the two resonant points are eliminated and filter no longer contains resonant points at low frequency range. The designed input filter PCB board is shown at Figure 5-8 and its measurement results are shown at Figure 5-9:

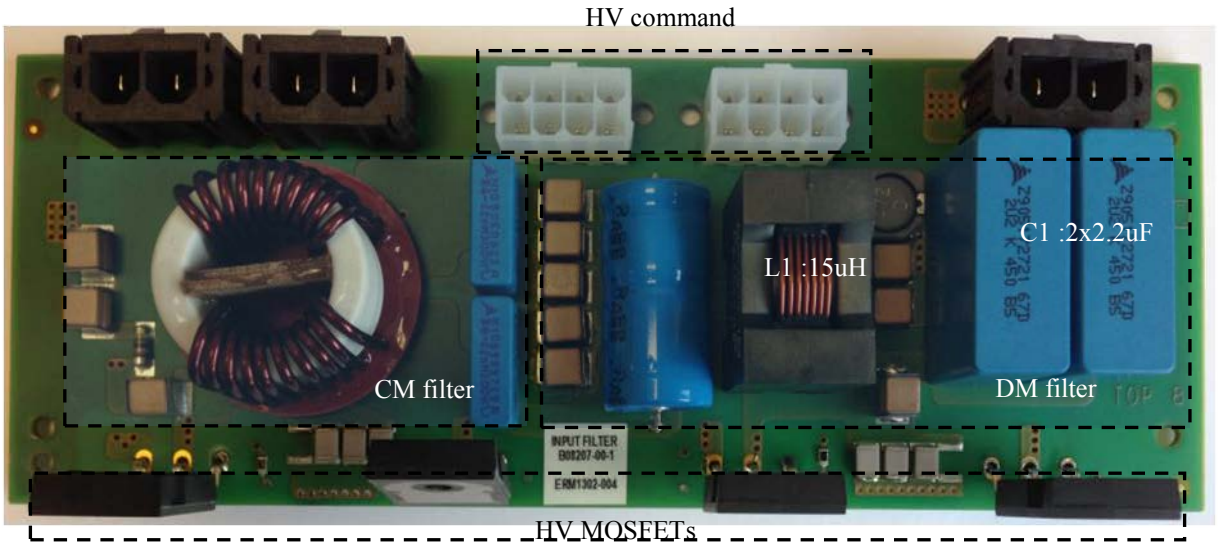


Figure 5-8. PCB board design of input filter

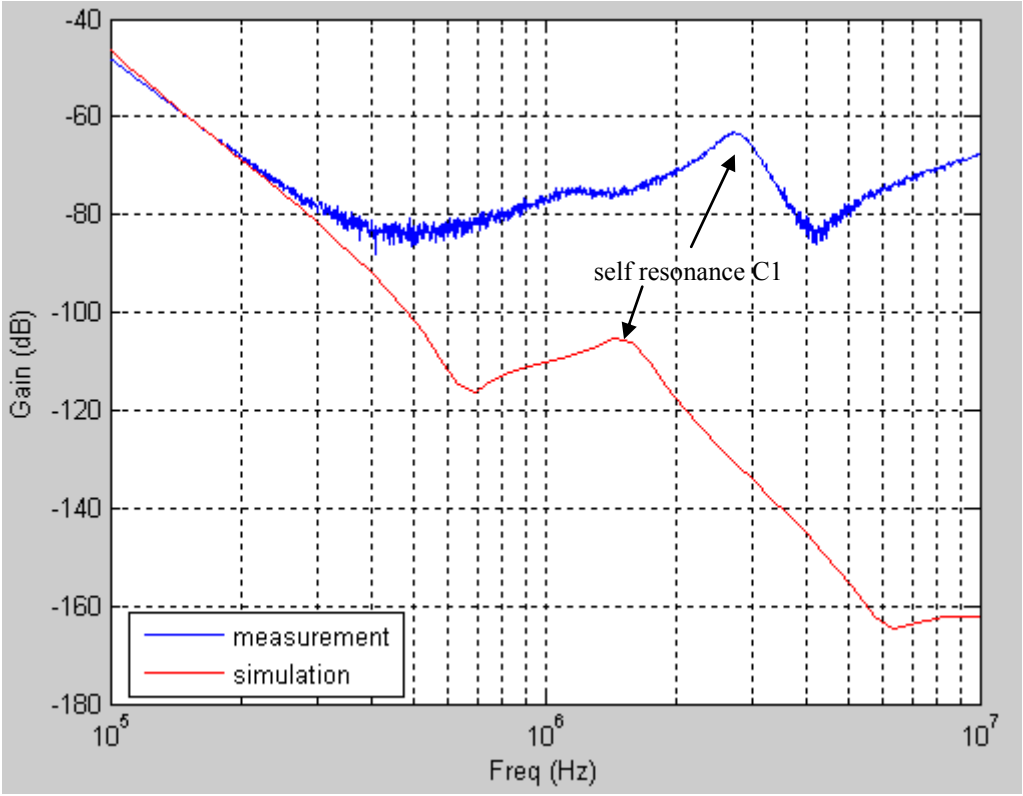


Figure 5-9. Simulation results considering components parasite and experimental results of input filter

Globally, the experimental results are in accordance with the simulation results up to the targeted emission frequency range: -77dB in experimentation for 300kHz. The effects of parasite elements become important when frequency continues to increase and filter's gain does not continue to decrease. A resonant frequency is detected at 3MHz. This is due to the parasite series inductance of the adopted film capacitor C1. The level of resonance is higher than simulated. Considering natural harmonic level reduction, the lower filter attenuation will not generate non compliance to EMC limits levels.

5.2.2 Output filter design and dimensioning

To achieve also high noise rejection, a Π filter solution is also selected at the secondary, shown as in Figure 5-10.

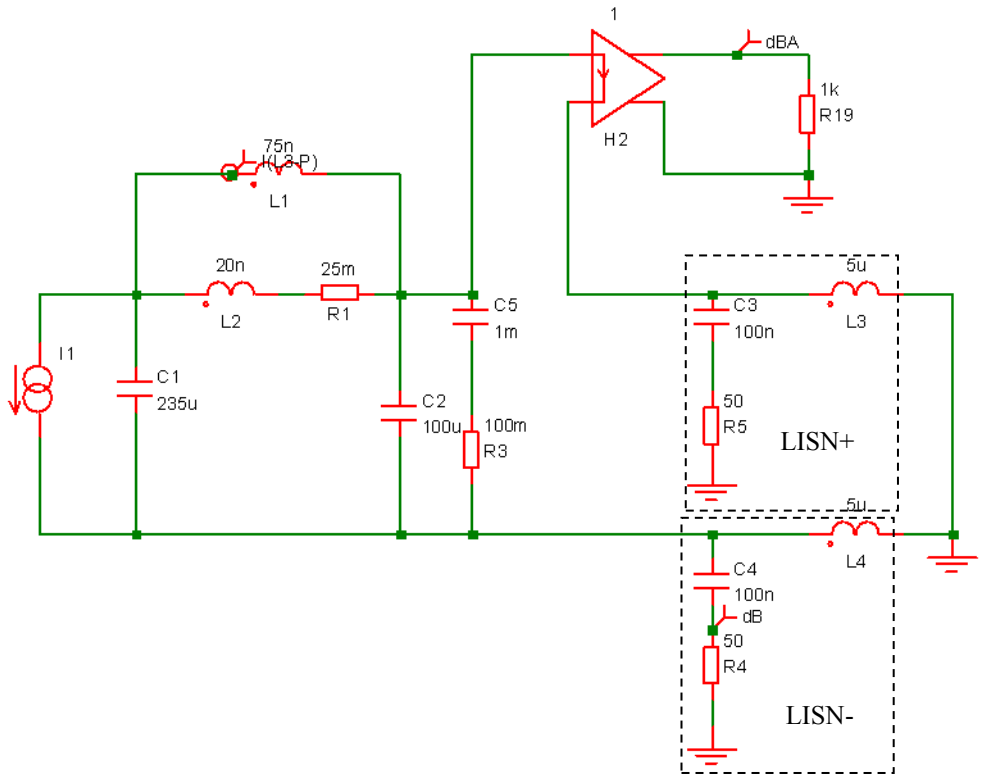


Figure 5-10. Proposed PI filter as output filter

Similarly, the basic Π filter is composed by C1, L1, C2 and L3+L4. L2 and R1 are used to damp the resonance between C1 and L1, the electrolytic capacitor C5 is adopted to damp the resonance between C2 and L3+L4. The output filter's PCB board is shown in Figure 5-10 and its performance is shown in Figure 5-11:

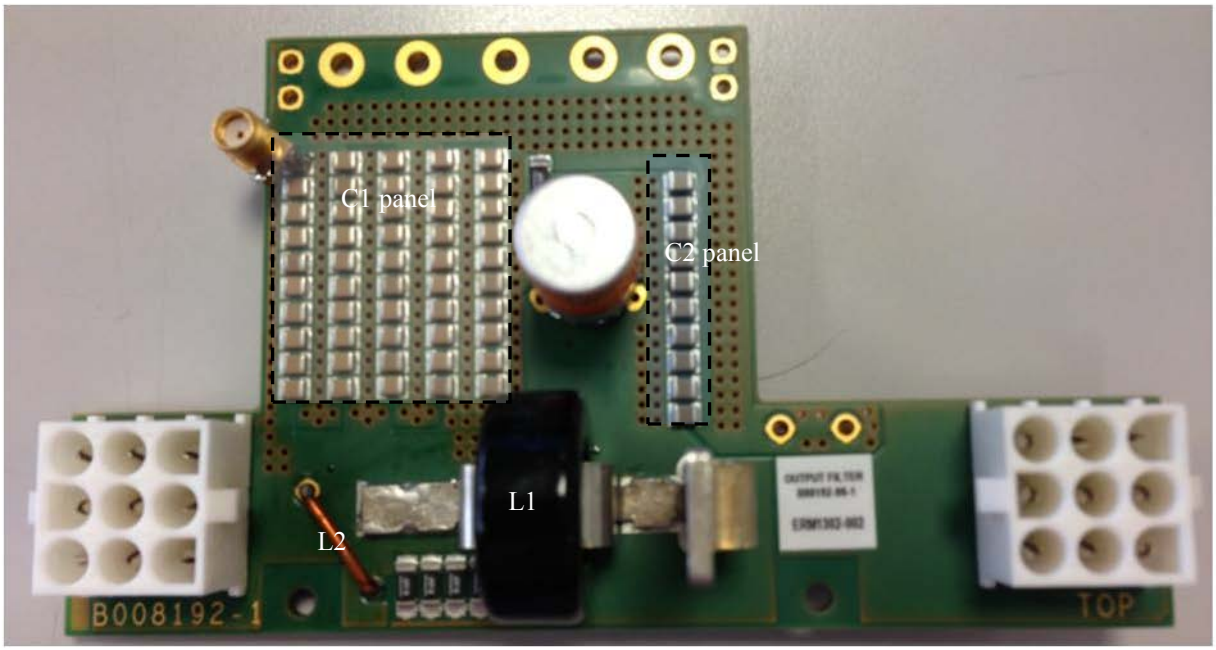


Figure 5-11. PCB board design of the output filter

The EMI choke L1 is made by a low permeability tore crossed by one conductor turn. The inductor L2 is simplified by using a 2cm length round copper wire of 2mm diameter.

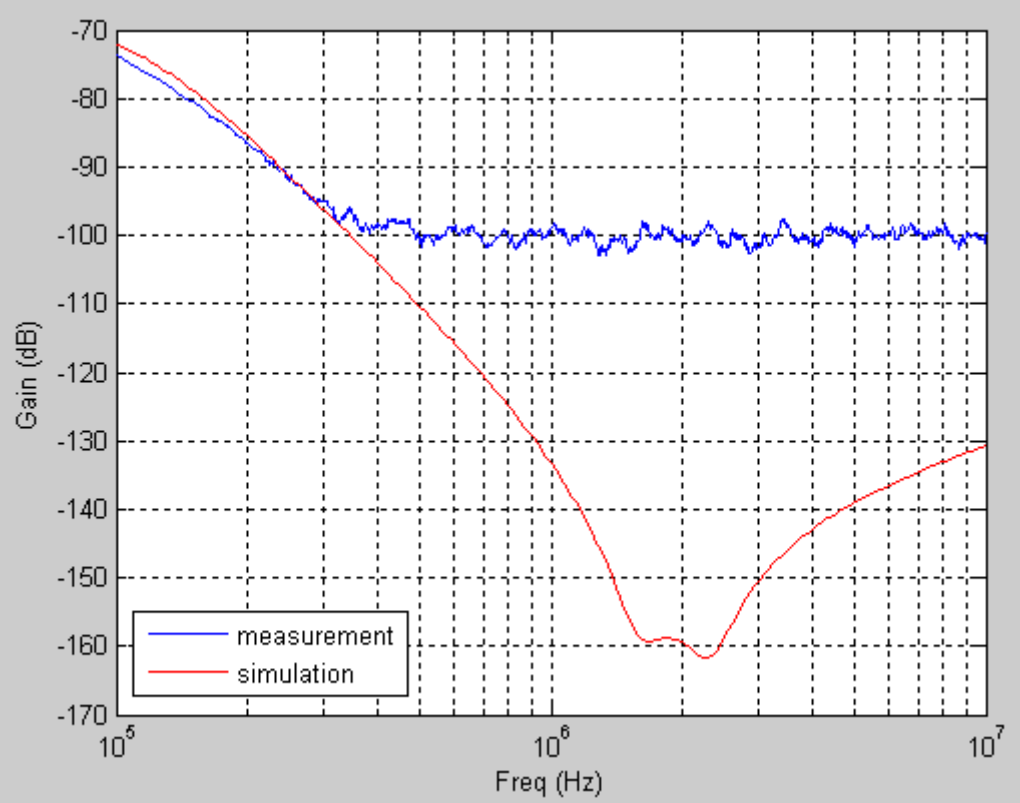


Figure 5-12. Simulation results considering components parasite and experimental results of output filter

As huge current ripples appear at output side, capacitor C1 and C2 are capacitor arrays to arrange high ripple: C1 is composed by 50x4.7uF ceramic capacitors in parallel, C2 is composed by 10x10uF ceramic capacitors in parallel. As ceramic capacitor has less parasite inductances than film capacitors, no resonance here is detected. The obtained gain at 300kHz is -95dB (the network analyzer can measure up to -100dB and limited to -100dB from then on).

5.3 Measurement results on conducted EMC and Discussions

To validate the effectiveness of designed filters, the conducted EMC of LLC converter is measured for single phase operation, double phase operation at Vin=330V and 410V, separately. The test bench for this EMC measurement and the measurement results are shown in the following parts:

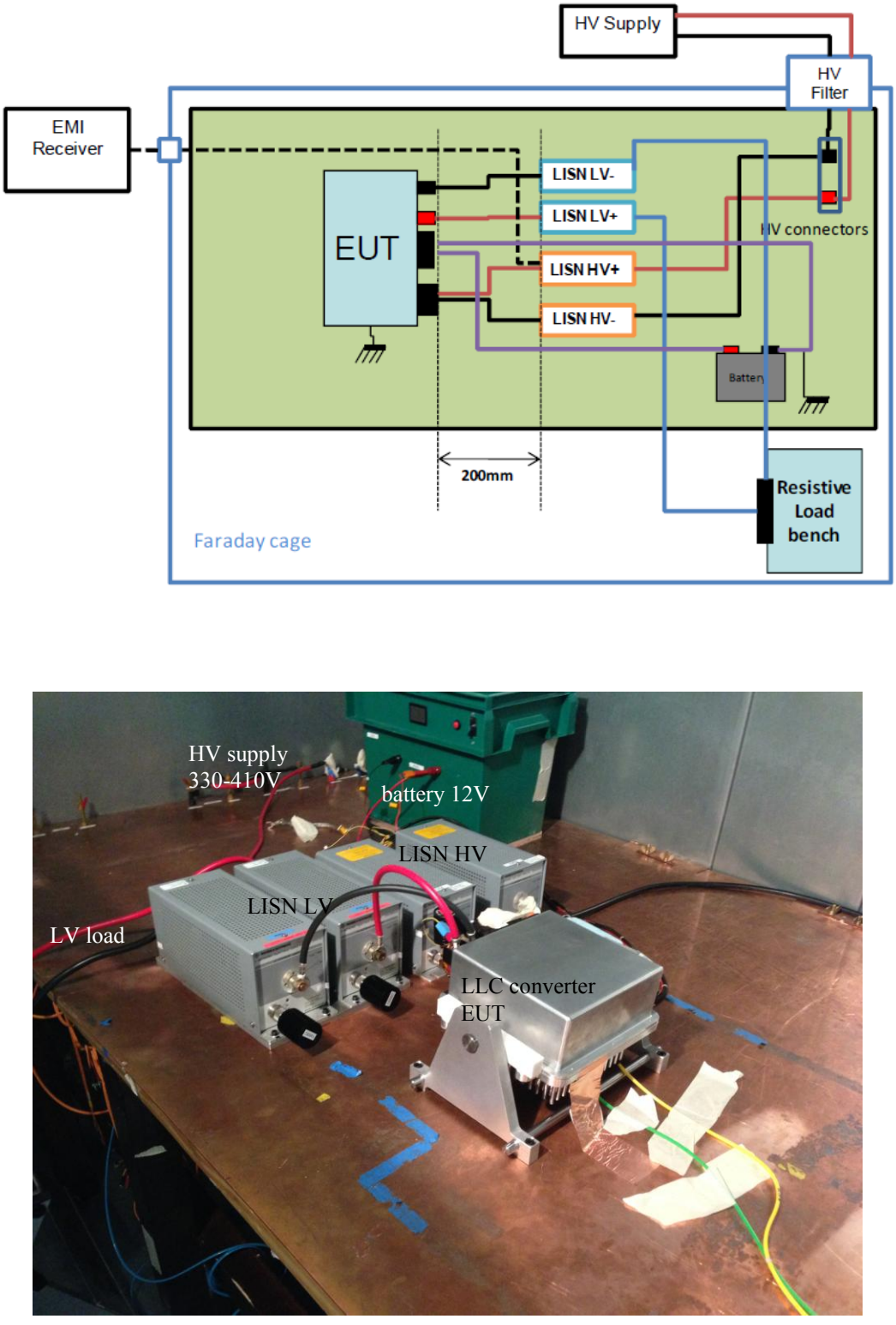


Figure 5-13. EMC measurement set up and its pictures

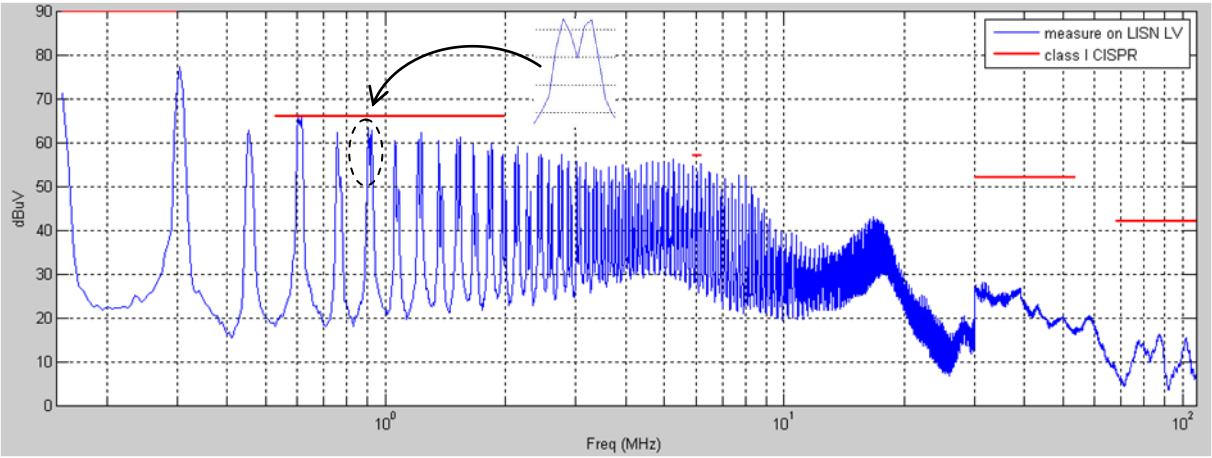


Figure 5-14. EMC conducted emission measurement at LISN LV (AVG detector, Vin=330V)

The main switching noise is detected at 2k*f*s frequencies. Transformer secondary asymmetries (current distributed not perfectly between two secondary windings of the transformer) cause additional noises at (2k-1)*f*s frequencies. Particularly for *f*s, the generated noise level is far less than that at 2*f*s, but as filters' attenuation at *f*s is 15dB less than 2*f*s, the noise at *f*s becomes significant in front of 2*f*s (72dBµV vs. 78dBµV). The asymmetries of transformer secondary windings should be precisely controlled in order to eliminate this noise.

As shown in Figure 5-14, for the fundamental and the first harmonic frequency it is not able to distinguish the difference of *f*a and *f*b due to the measurement resolution. Starting from the 5*f*s, the differences of two adjacent frequencies become apparent. The noises levels at adjacent frequencies are equal, verifying the discussed noise superposition in frequency domain. To further study the interferences between two power cells, an EMC measurement at low frequency range is done, shown as in Figure 5-15.

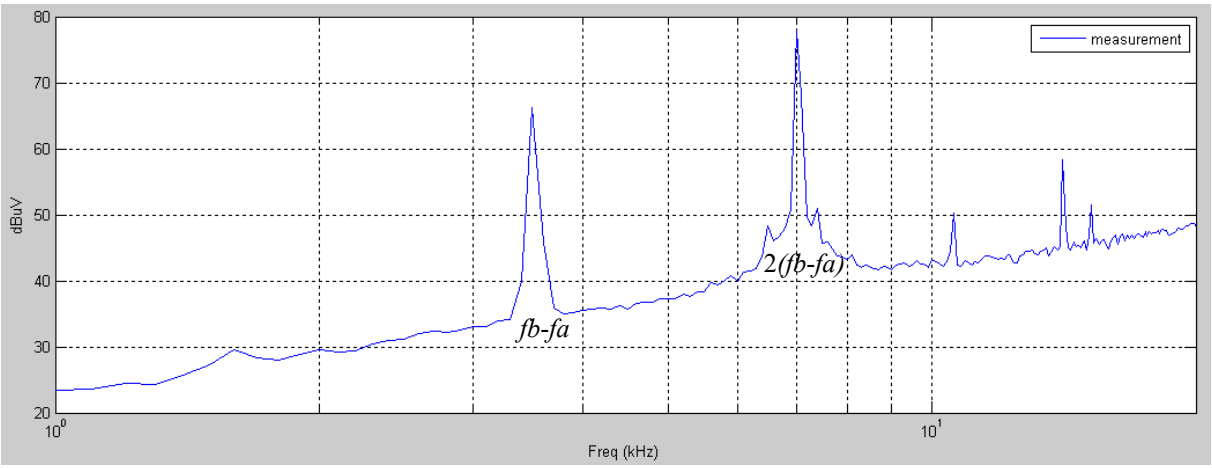


Figure 5-15. EMC measurement for low frequency at LISN LV+ (AVG detector, Vin=330V)

The main beat frequency 2(*f*b-*f*a) is measured at 78dBµV (76dBµV simulated) and another beat frequency (*f*b-*f*a) appears due to transformer asymmetries. As the beating noise is very limited, it will not influence the correct circuit converter operation behavior.

Different EMI limits applicable to HV battery as it allows higher levels of conducted emissions than LV battery [5-4, 5-5]. The measurement results are shown at Figure 5-16.

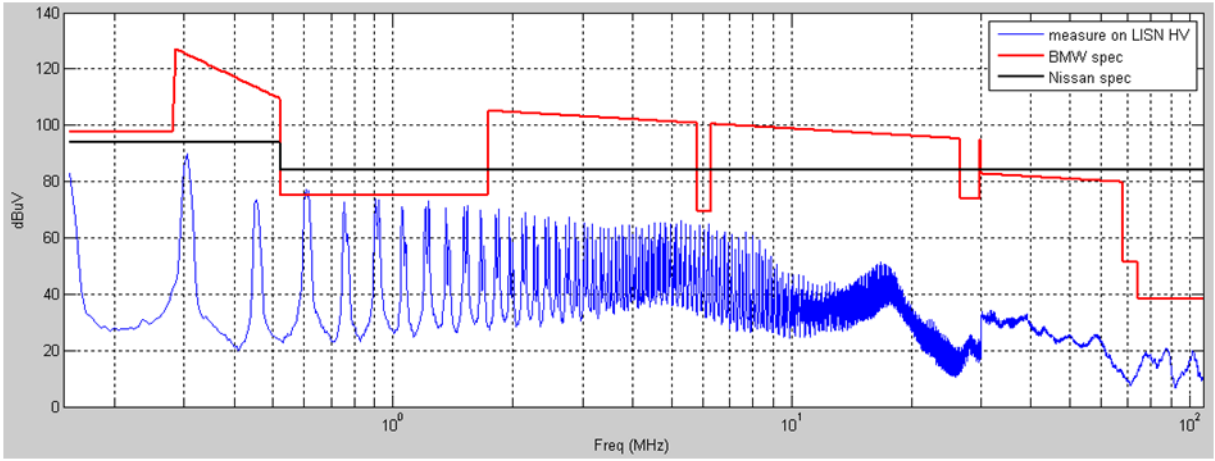


Figure 5-16. EMC conducted emission measurement at LISN HV+ (AVG detector, Vin=330V)

As reported in Figure 5-16, almost all the noises are kept under the specified limits. The noise for 4*f*s is slightly above the defined limit. This is because that the input filter performs lower attenuation for this frequency as reported in Figure 5-9. Improving the circuit board layout can effectively reduce the noise.

5.4 References:

[5-1] Mao Zhang, Weiping Zhang and Zheng Zhang, "Study of high frequency input interference for Buck converter", PIERS Proceedings, pp. 1126-1131, Cambridge USA, July,2010

[5-2] Juanjuan Sun, "Dynamic performance analysis of current sharing control for DC/DC converters", PhD thesis of Virginia Polytechnic Institute and State University, 2007

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Chapter 6. Conclusions

This dissertation verifies LLC structure as a good candidate to realize efficient DC/DC HV/LV power conversion in automotive industry. The reported performance of this converter prototype shows its advantages in terms of efficiency improvement, volume miniaturization and EMI reduction than other available topologies.

This thesis proposes a new LLC converter designing procedure to ameliorate the circuit electrical parameters. In this procedure, secondary leakage inductance's effect to the LLC's characteristics is analyzed in detail and it is verified that its effect cannot be neglected when secondary resistance is low. To exhibit ZVS at HV MOSFETs, the dead-time selection should consider the effects of nonlinear output capacitance characteristics of MOSFETs. To obtain high power capacity while keeping a large input variation range, double stage LLC with BOOST as an input-stage power factor corrector is verified to be a better solution than single stage LLC. LLC converter should be designed to offer high efficiency between [330V 410V], and a BOOST stage is designed to broaden the input variation range.

The proposed double cell parallel arrangement to handle 180A output current is able to keep a high efficiency at a wide load range. High efficiency at light load is assured by switching off one power cell. In order to avoid the current dissymmetry problems in parallel interleaving LLC, proposed double loop control strategy can equalize the current distribution between two power cells. Regulation parameters can be designed by the aid of Simplis simulation software to obtain both stability and rapidity at current/voltage control loops.

This work also proposes many new implementations for improving the performance of LLC converter. Transformer with E structure integrating magnetizing inductor and partial resonant inductor is verified to be a good solution to get a compact magnetic integration. The Litz wire is a good solution implemented to reduce eddy current loss but its strand diameter should be carefully selected and should be kept away from air-gap. LV MOSFETs in IML module proved its effectiveness in reducing thermal resistances and it is a good solution to handle high output current conduction loss. The air-cooling system with vapor-chamber as heat spreader is effective in rapid and homogenous heat spreading.

Double cell LLC with equal current distribution has two operational frequencies close to each other. The dimensioning of input/output filter can be simplified by considering the noises of only one cell; the other cell at adjacent frequency beneficed the same damping naturally. To

allow a stable operation of double cell LLC, low frequency beatings should be filtered by bypass capacitors close to each power cell.

Considering the future work, the converter can be further improved in the following aspects: Firstly, since double stage LLC is highly preferred than single stage LLC, it is interesting to study the possibility to operate the LLC at its load independent point with a fixed frequency, while the duty cycle of BOOST is controlled to regulate the output voltage. As the LLC works at a fixed frequency, its secondary rectification keeps the same frequency as primary driving signal and thus can be greatly simplified. Secondly, the transformer's secondary leakage inductance should be minimized to reduce conduction loss and reduce the spike voltage. The reverse recovery loss can be avoided and additionally, the secondary snubber is no longer indispensable (snubber loss can be further reduced). Thirdly, for the final industrialized version LLC, it is possible to keep all the magnetic components in the original three-element structure, while all the inductances or transformers can be realized by planar magnetic cores. The total magnetic component number is thus increased but considering that the planar structure has a larger dissipation area and a possibility for winding within PCB board, it may be a good solution for industrializing the prototype's magnetic components.